

# PG150-C03

384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

## TABLE OF CONTENTS

Page Description

1	Table of Contents
2	BLOCK DIAGRAM
3	PCI EXPRESS
4	PCIE TERM
5	MEMORY: GPU PARTITION A/B
6	MEMORY: FBA PARTITION[31:0]
7	MEMORY: FBA PARTITION[63:32]
8	MEMORY: FBB PARTITION[31:0]
9	MEMORY: FBB PARTITION[63:32]
10	MEMORY: GPU PARTITION C/D
11	MEMORY: FBC PARTITION[31:0]
12	MEMORY: FBC PARTITION[63:32]
13	MEMORY: FBD PARTITION[31:0]
14	MEMORY: FBD PARTITION[63:32]
15	MEMORY: GPU PARTITION E/F
16	MEMORY: FBE PARTITION[31:0]
17	MEMORY: FBE PARTITION[63:32]
18	MEMORY: FBF PARTITION[31:0]
19	MEMORY: FBF PARTITION[63:32]
20	GPU PWR AND GND
21	GPU PWR, GND and NCs
22	GPU DECOUPLING
23	GPU DECOUPLING 2
24	IFPA/B DP
25	IFPE DP

Page Description

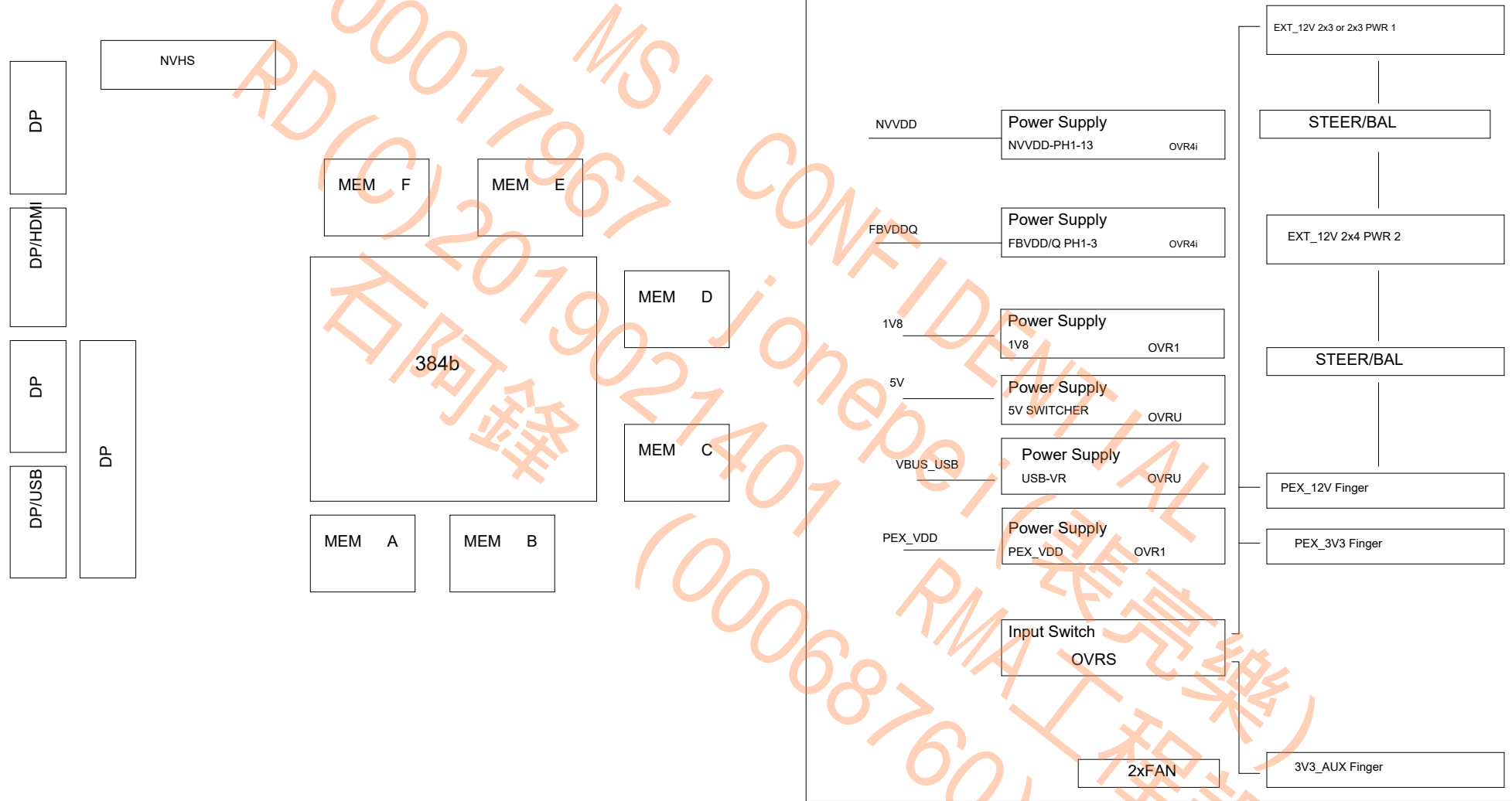
26	IFPF USB
27	IFPC HDMI/DP
28	IFPD DP
29	NVHS X16
30	MISC: THERMAL, JTAG, GPIO, STEREO
31	MISC: ROM, STRAPS
32	MISC: XTAL, PLL
33	MISC: USB PPC
34	PS: USB_C VR
35	PS: 5V
36	PS: PEXVDD 1V8 Rail
37	PS: FBVDD Controller
38	PS: FBVDD Controller OVR3
39	PS: FBVDD Phase 1, 2
40	PS: FBVDD Phase 3
41	PS: NVVDD Controller_OVR8
42	PS: NVVDD Phase 1
43	PS: NVVDD Phase 2
44	PS: NVVDD Phase 3, 4
45	PS: NVVDD Phase 5
46	PS: NVVDD Phase 7, 8
47	PS: NVVDD Phase 9, 10
48	PS: NVVDD Phase 11, 12
49	PS: NVVDD Phase 13, 14
50	PS: INPUT SWITCH_RTD3

Page Description

51	PS: INPUT SWITCH_RTD3 USB
52	PS: INPUT SWITCH RAIL BALANCE
53	PS: DISCRETE STEERING
54	PS: Input, filtering, and Monitoring
55	PS: Current Sterring, Hot Unplug
56	PS: Prefilter
57	Sequence: 5V, 1V8, NV3V3 EN
58	Sequence: NV, PEX, FB EN
59	Sequence: PCIe Voltage Monitor
60	Sequence: Discharge
61	Sequence: MISC
62	MISC: FAN & LED1
63	MISCL: LED 2
64	MCU ZERO POWER IDLE
65	MECH
66	VR Thermal Protection



Block Diagram







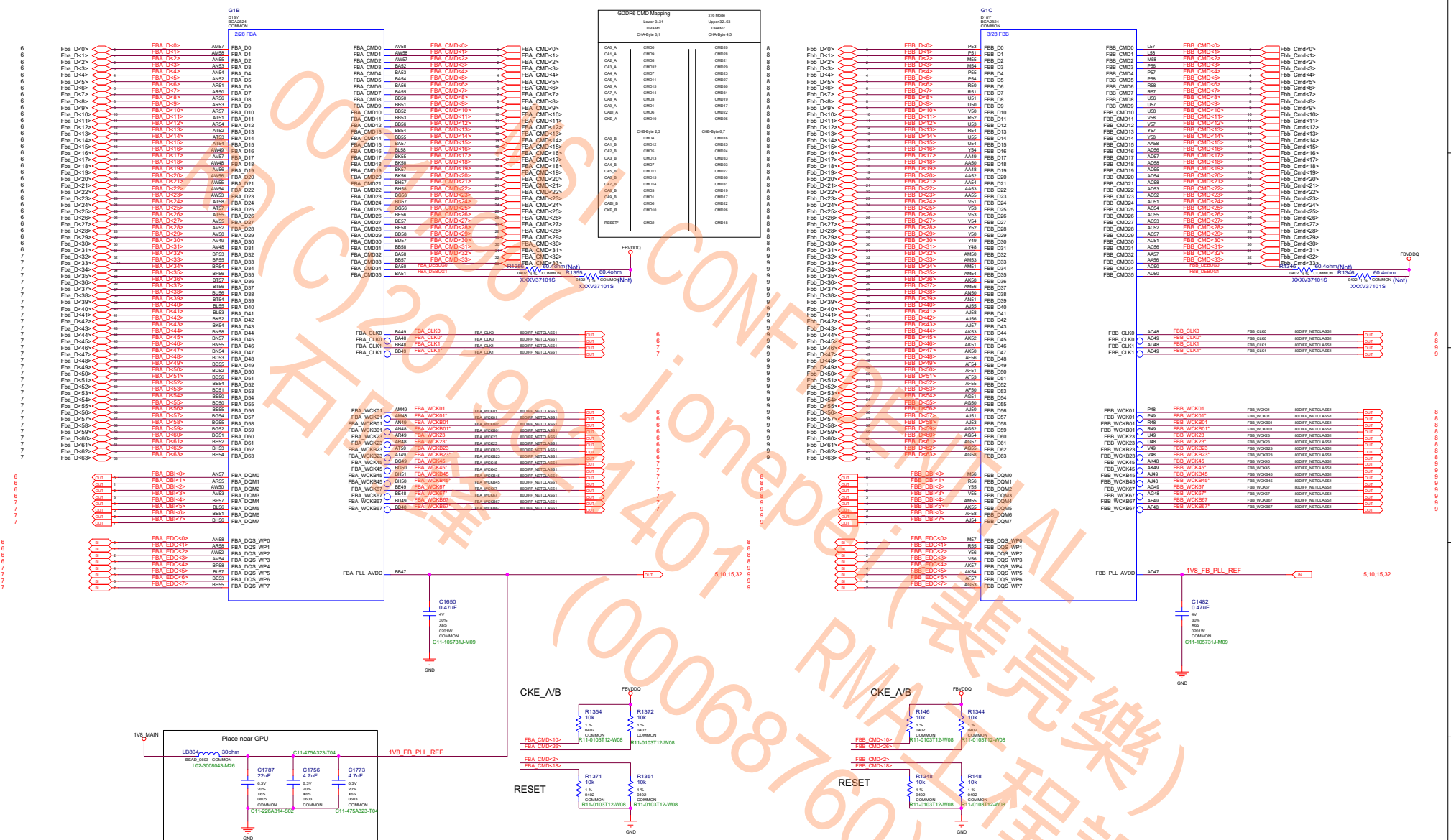


PCI TERM



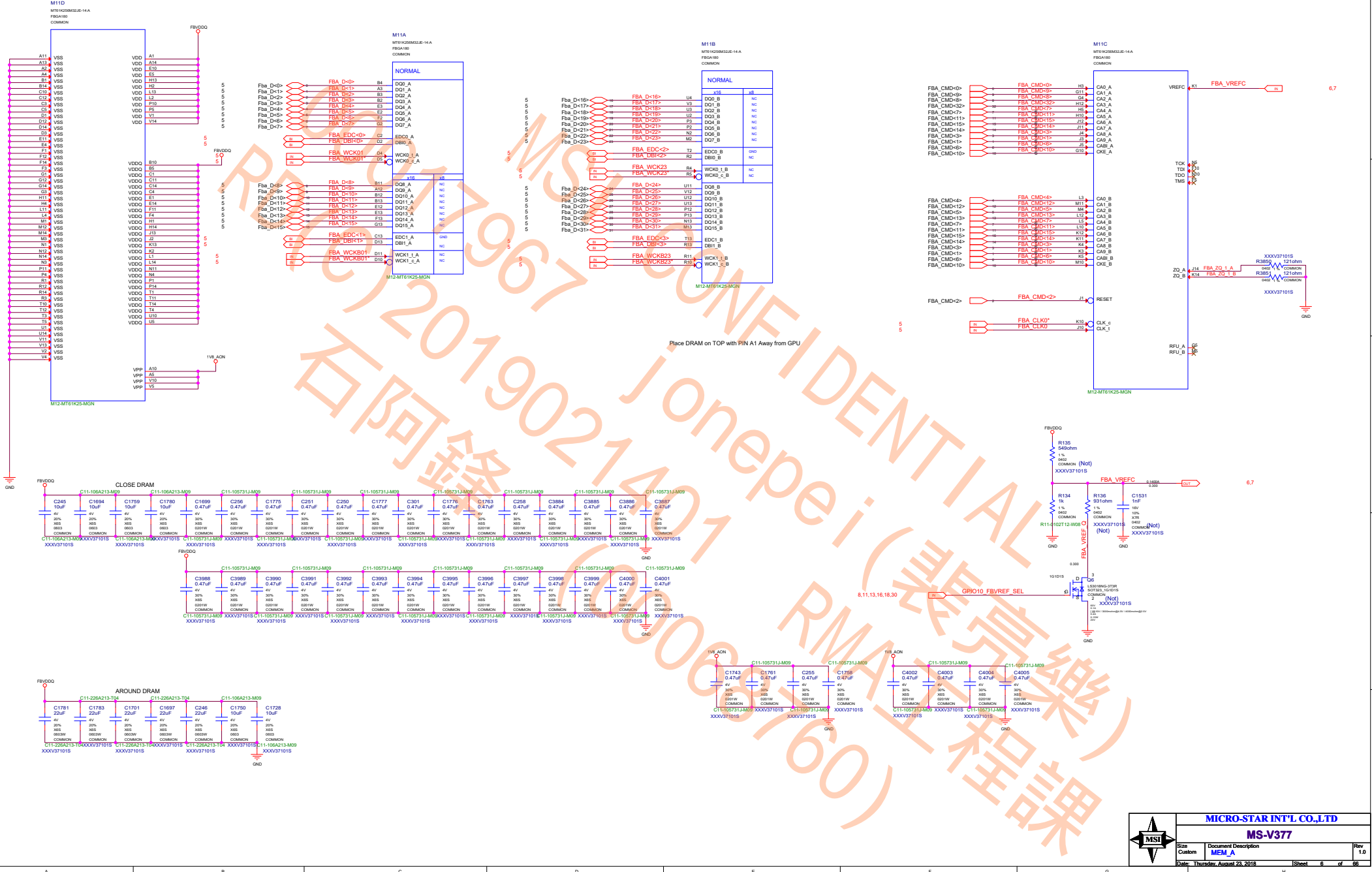


MEMORY: GPU Partition A/B

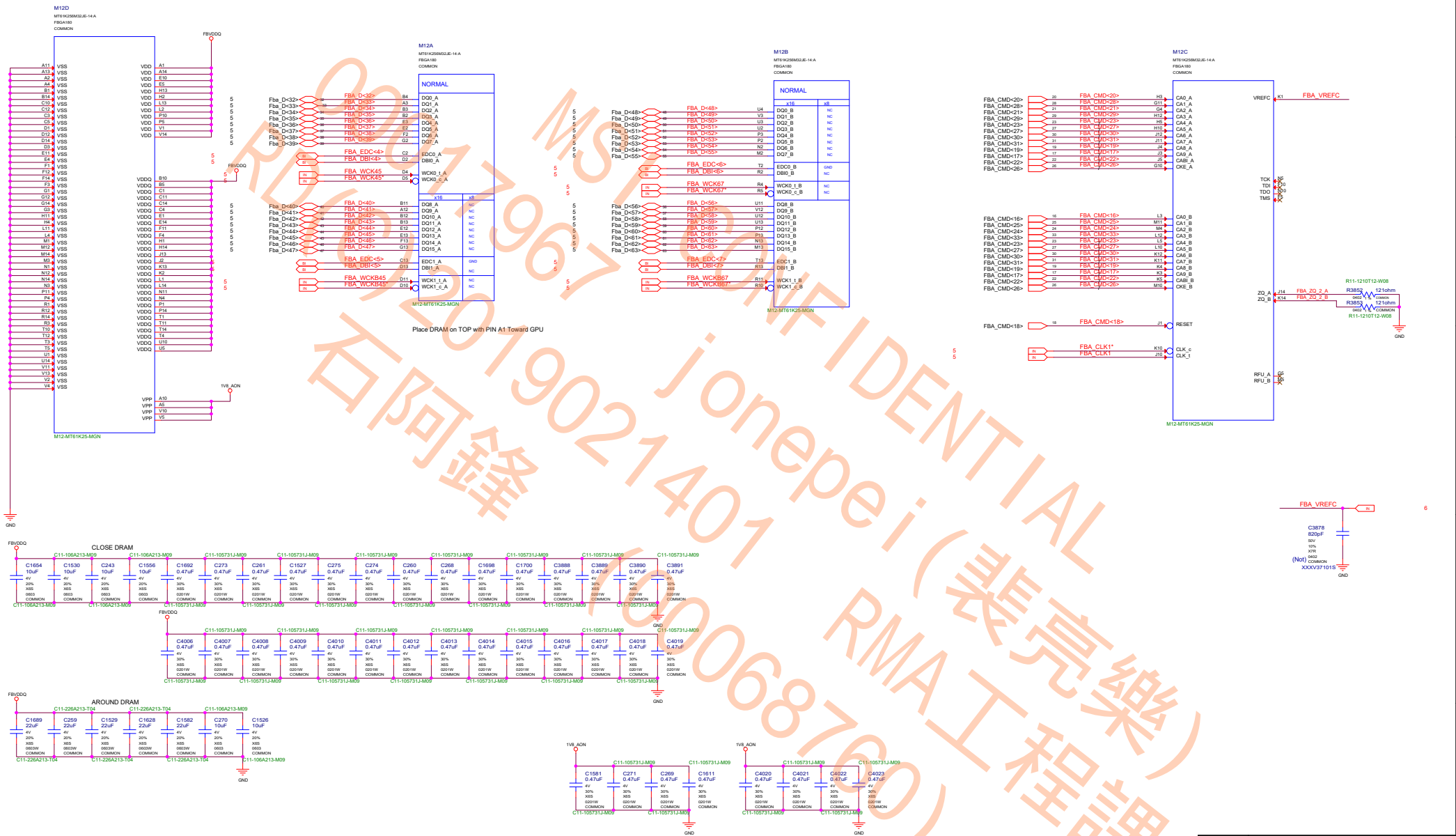




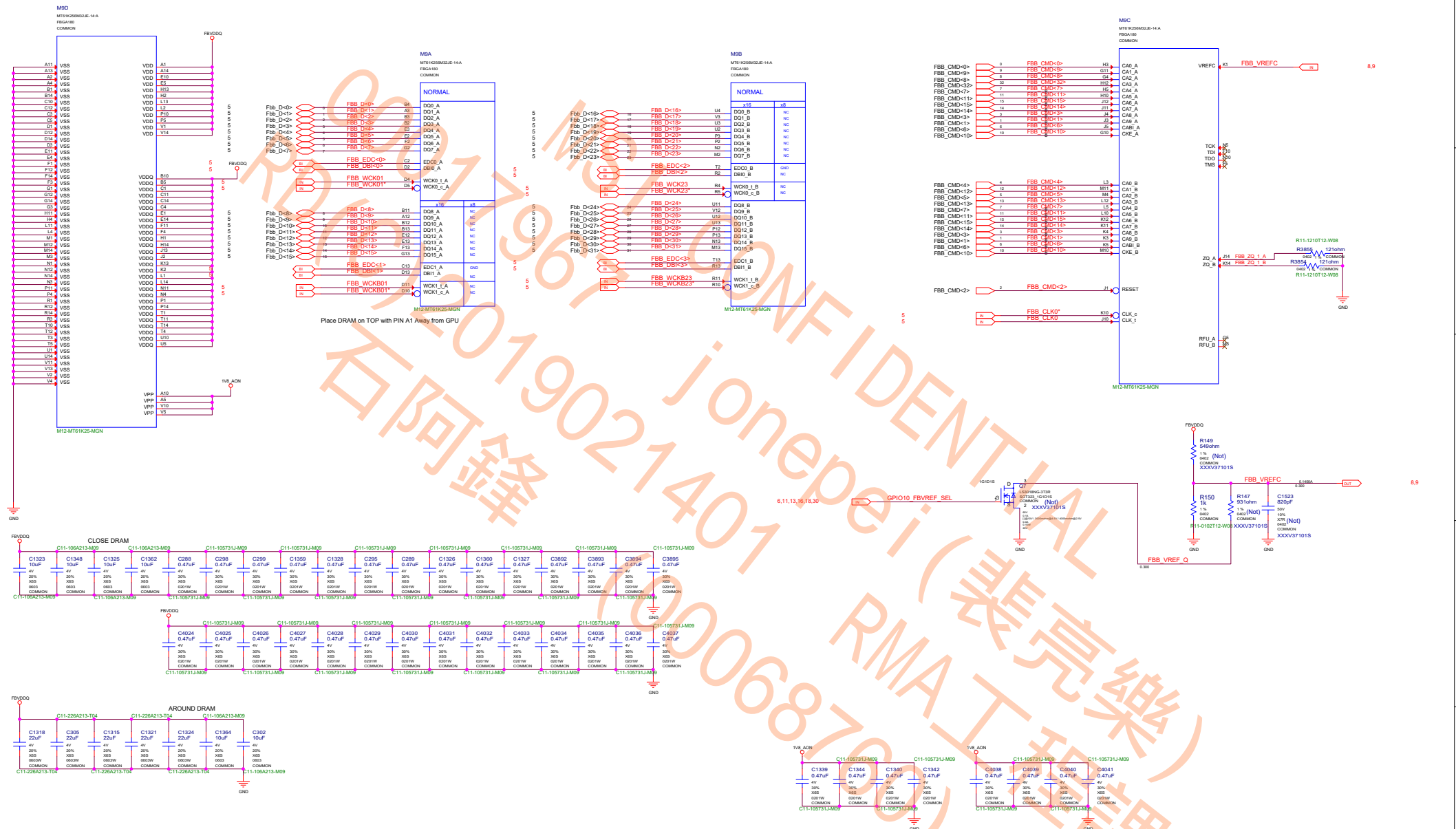
# MEMORY: FBA Partition 31..0



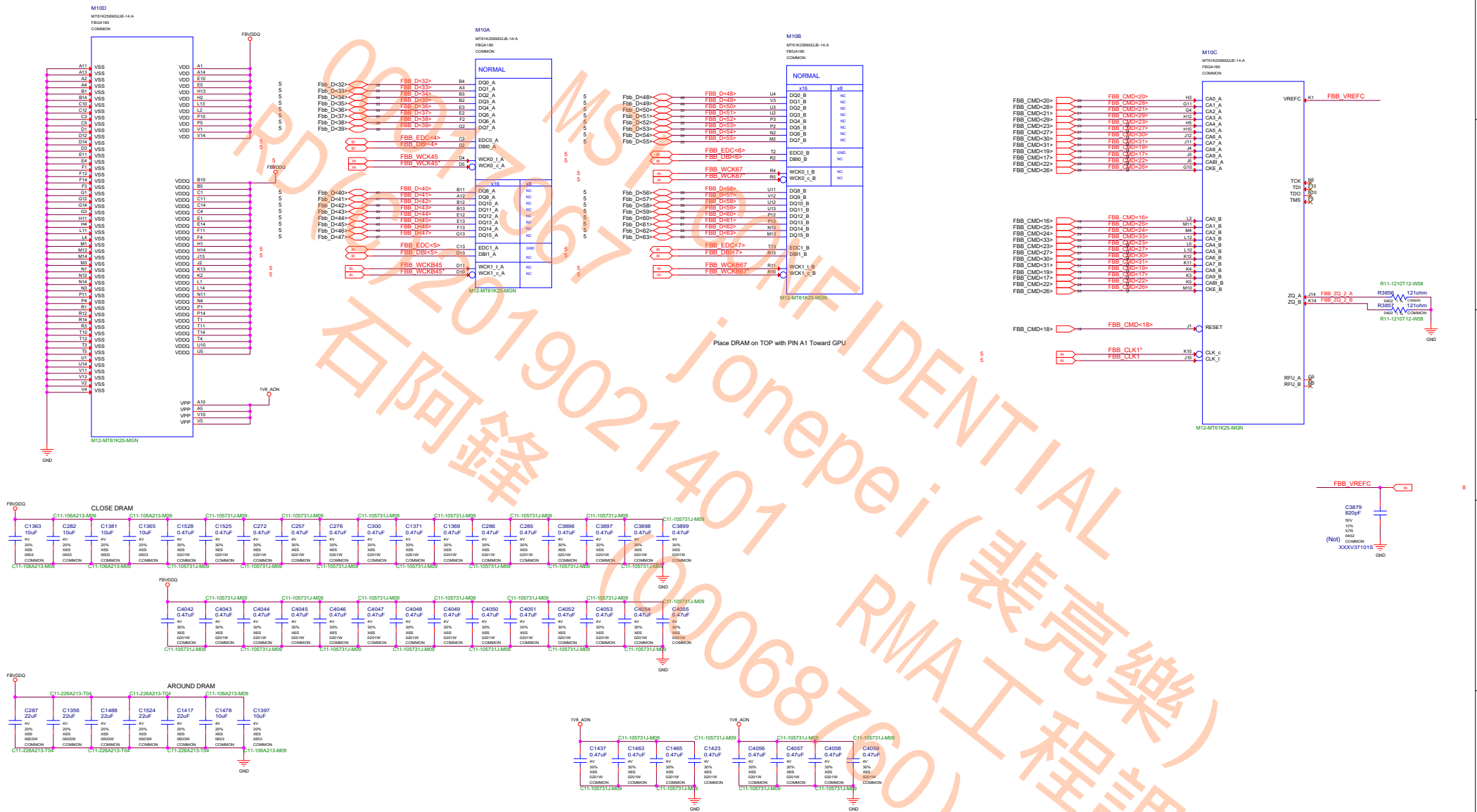




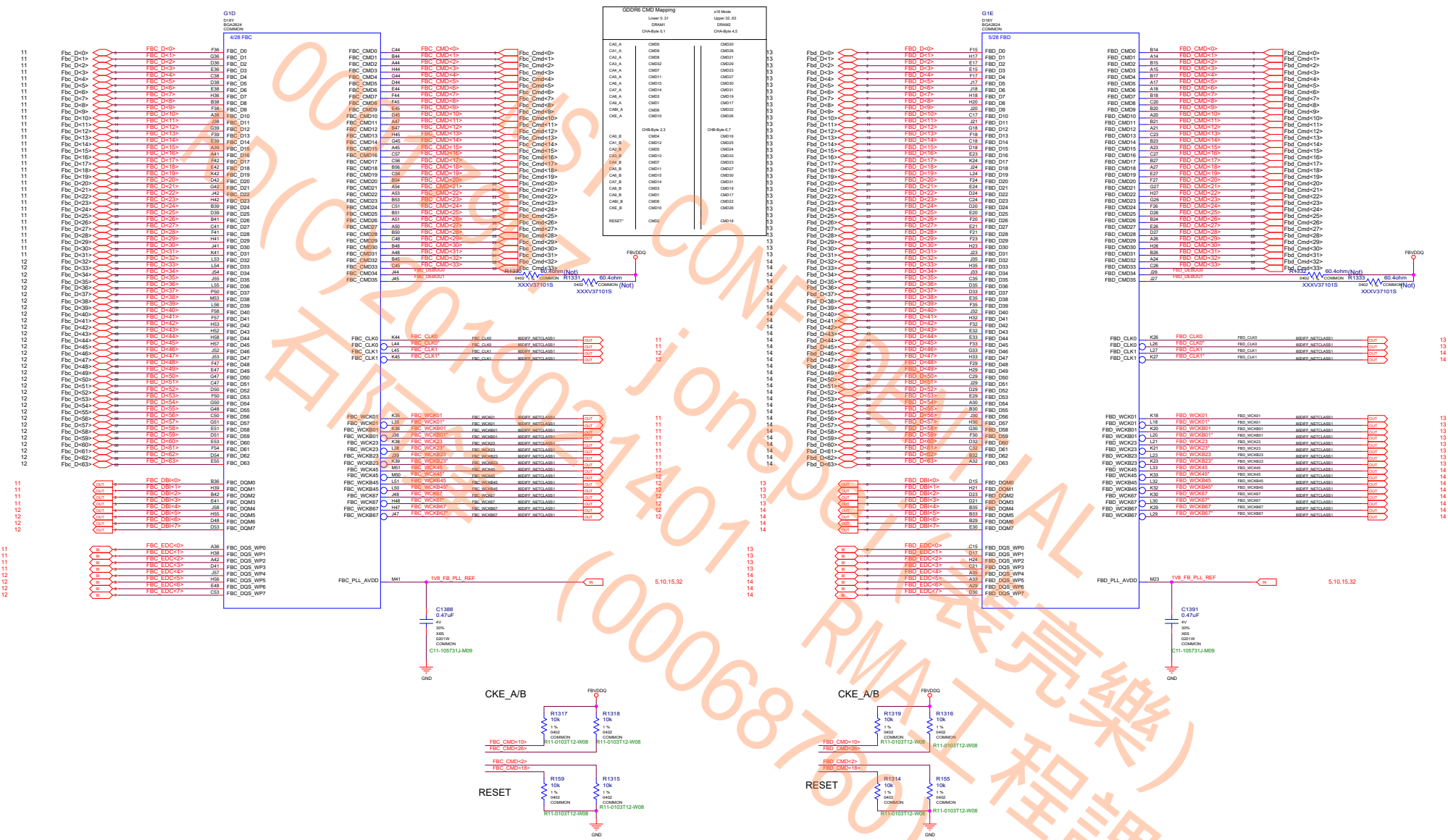






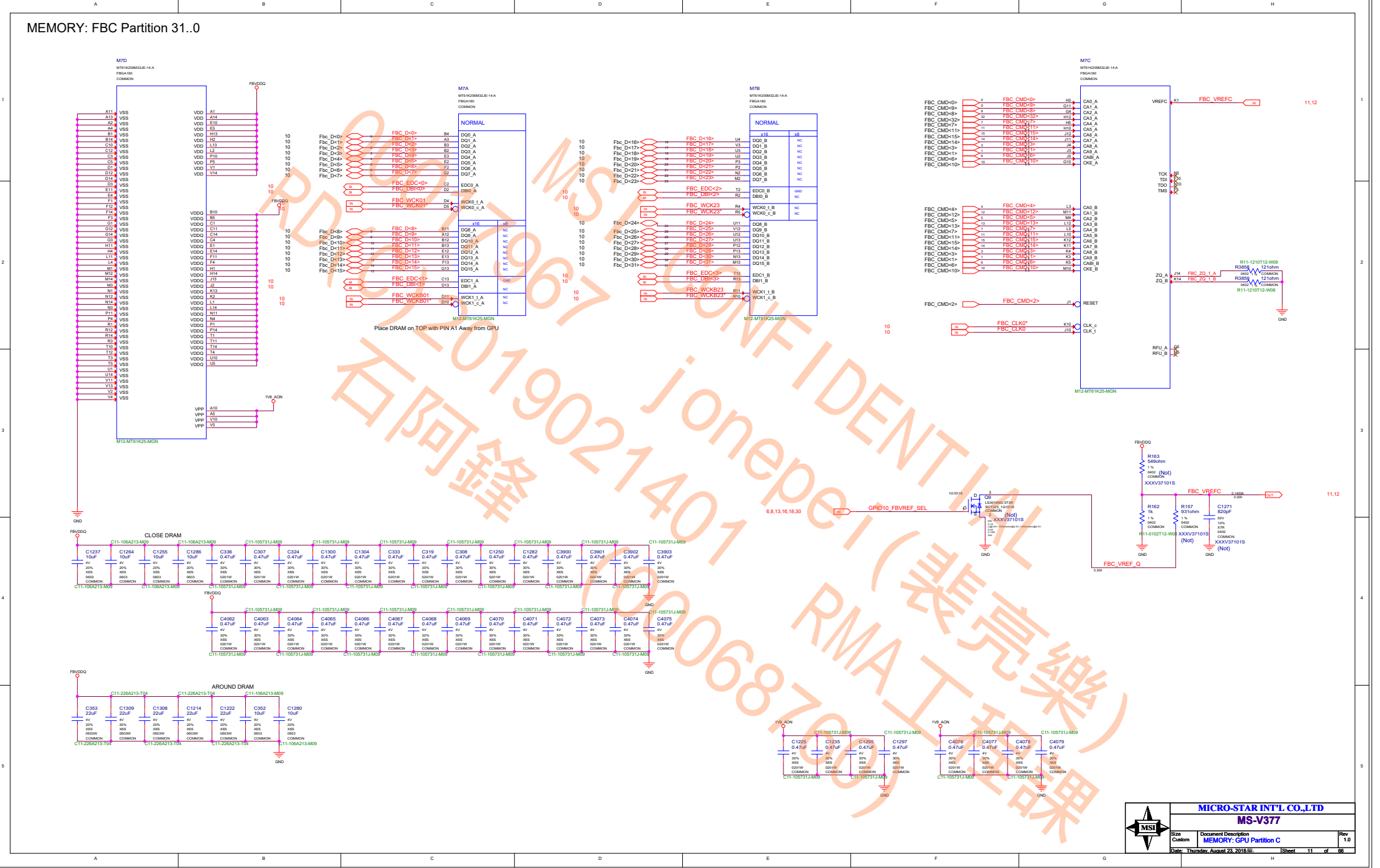




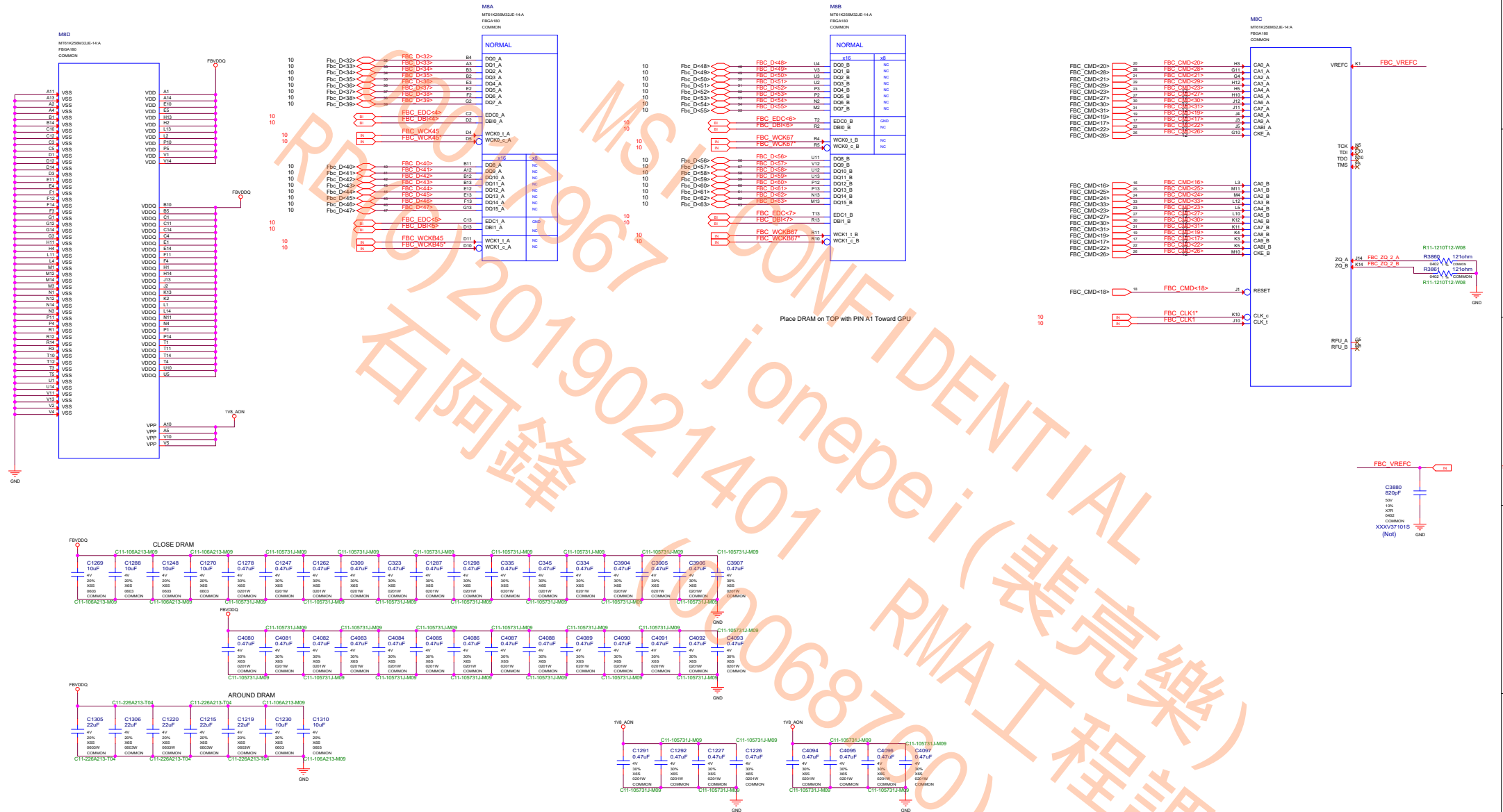




MEMORY: FBC Partition 31..0

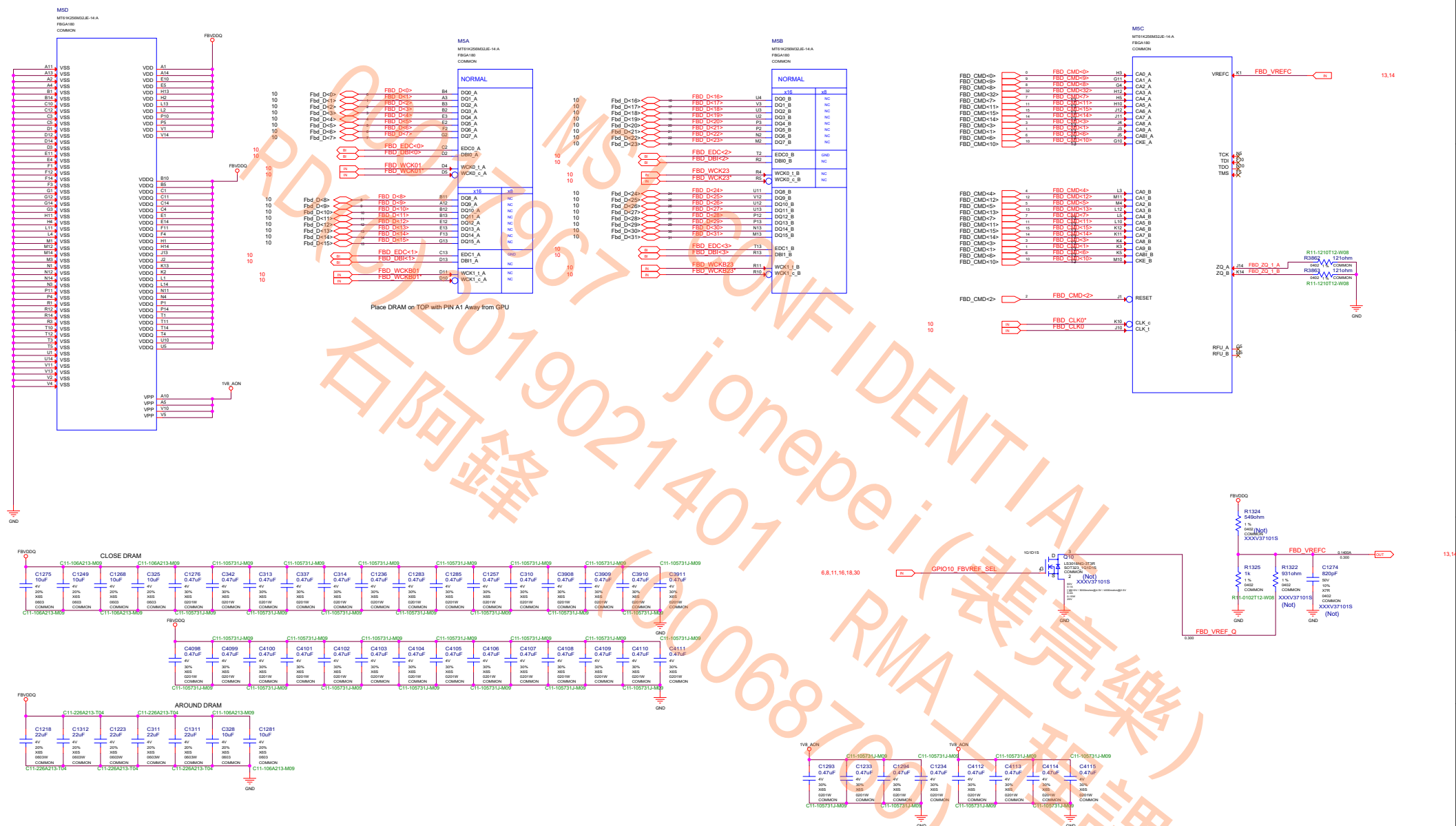




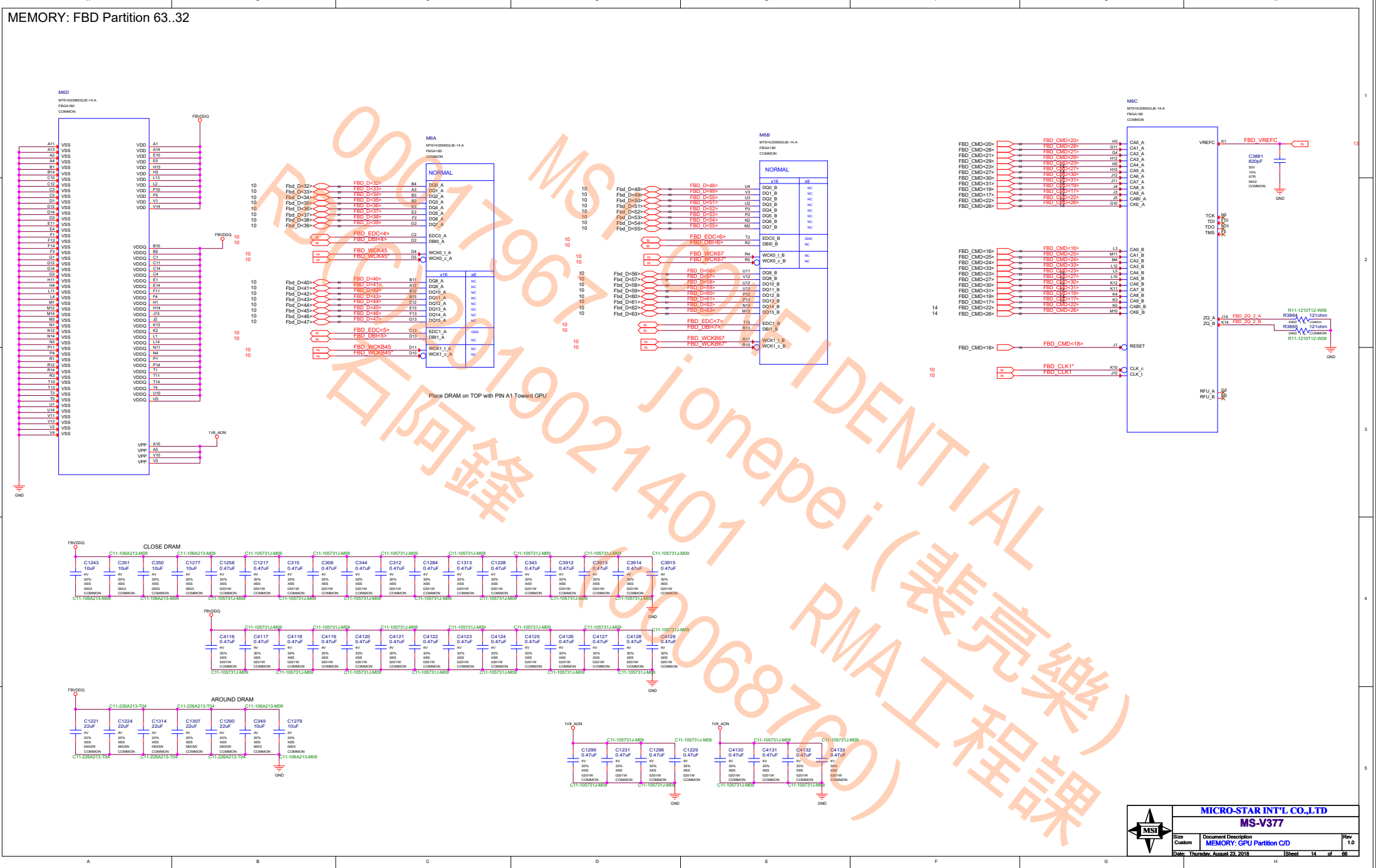




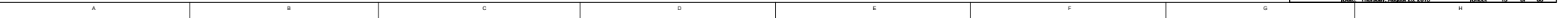
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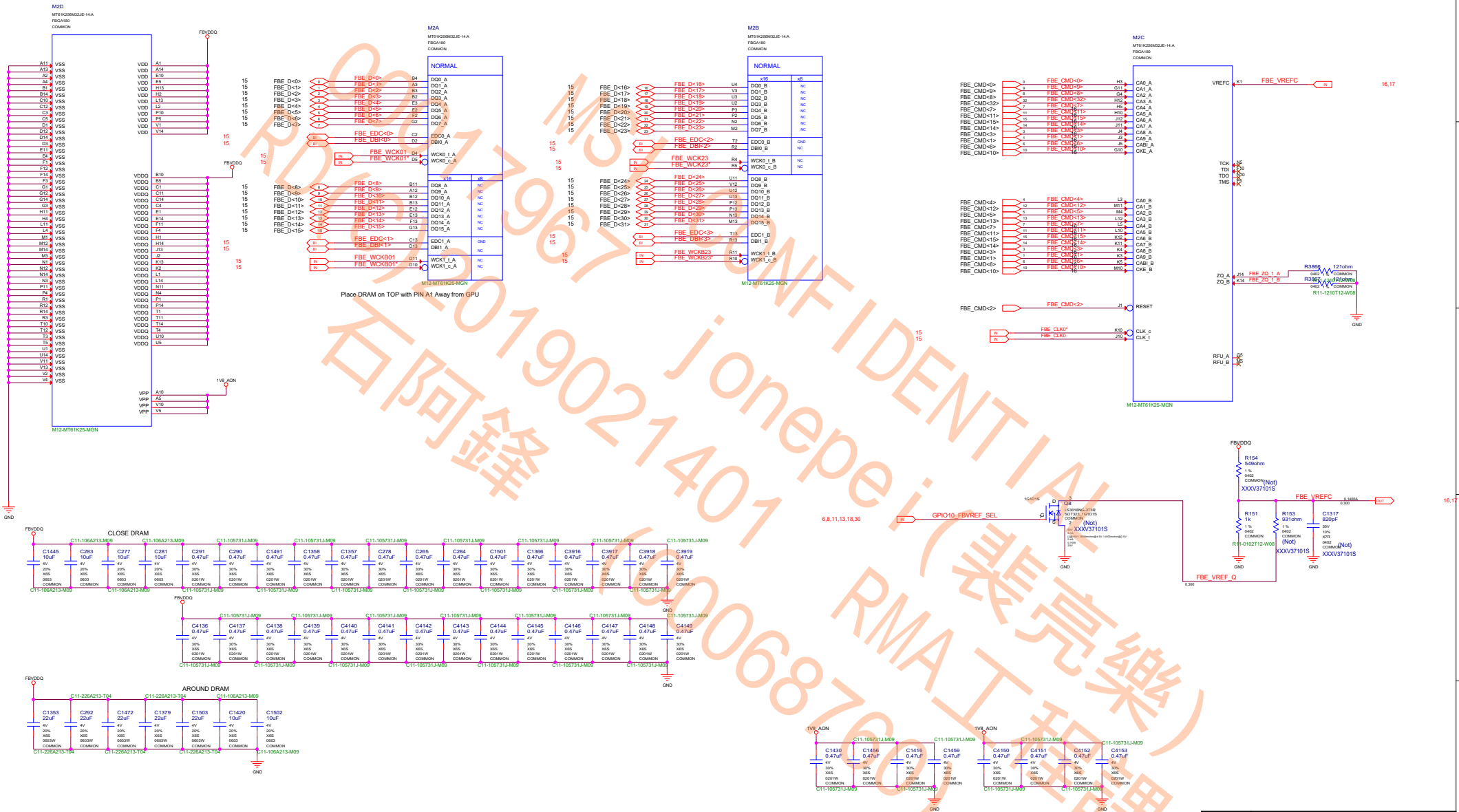




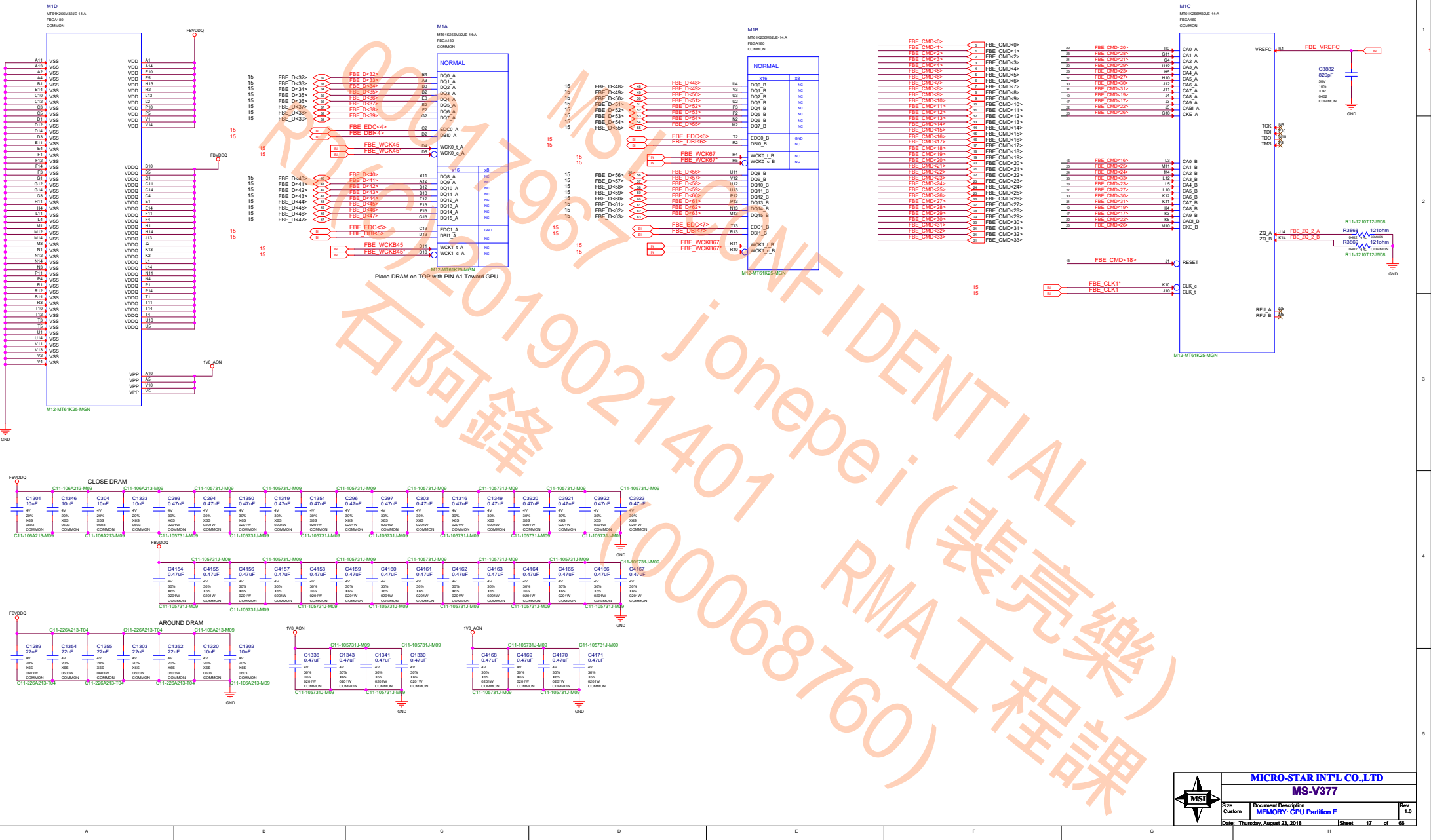




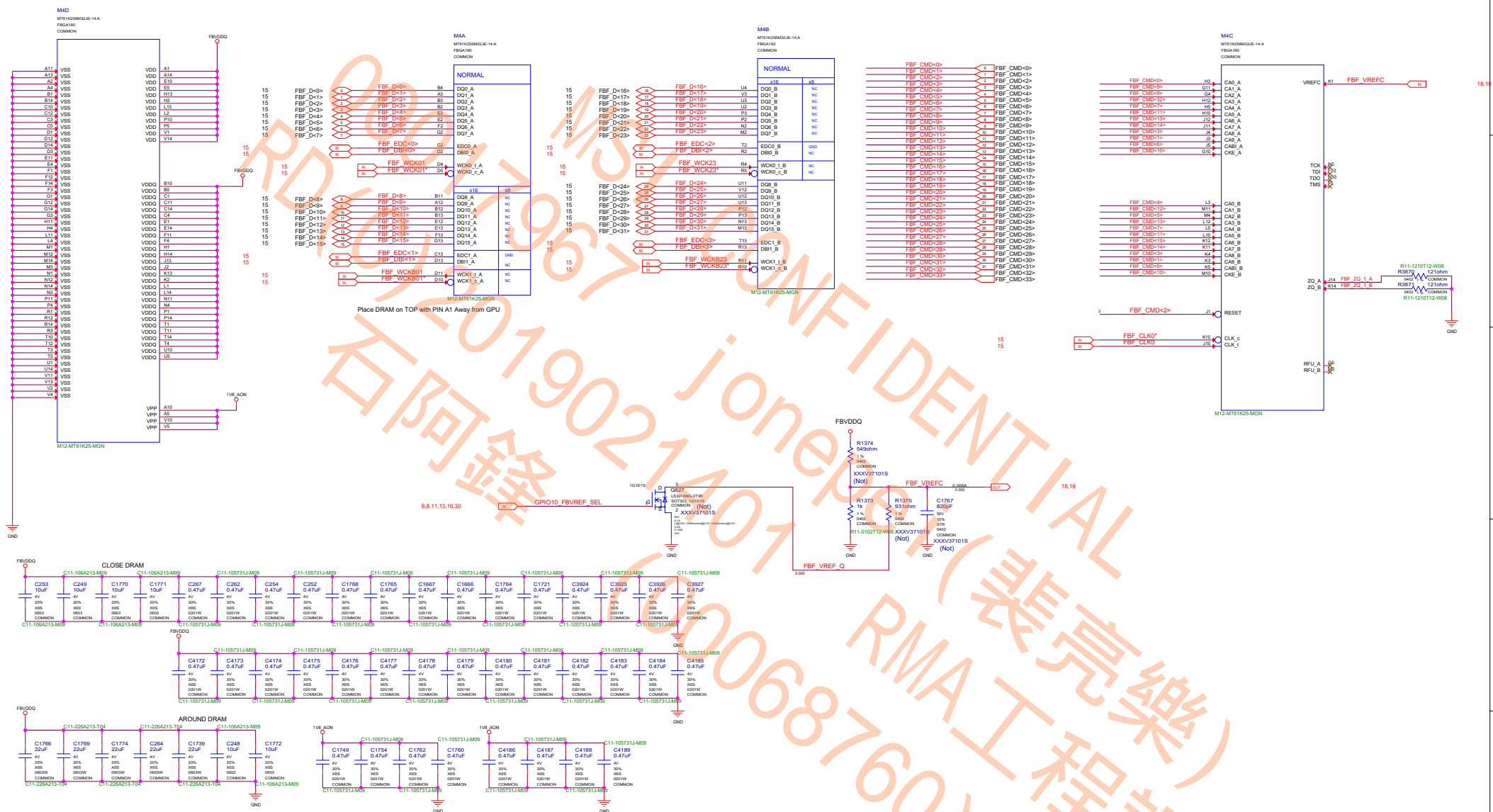










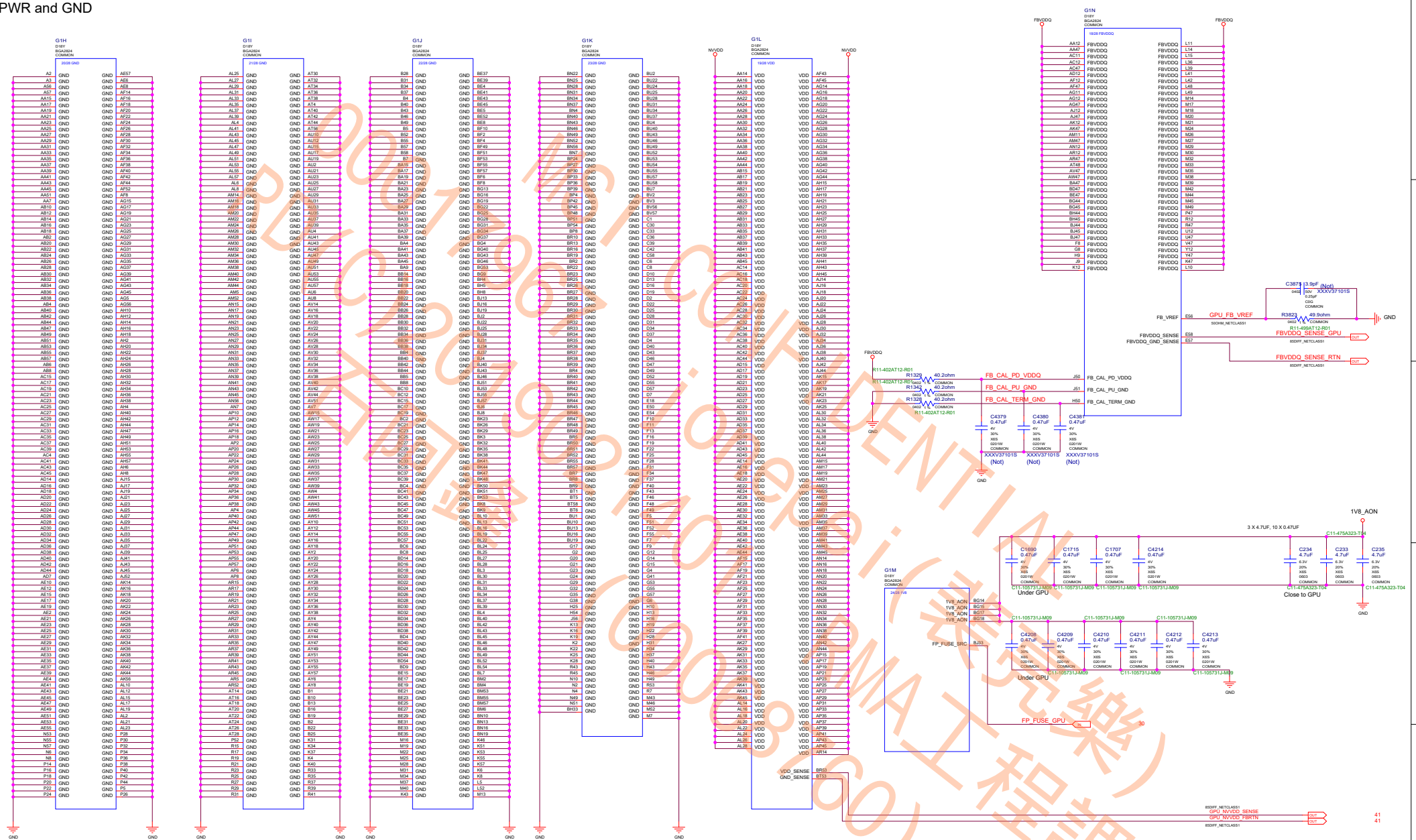






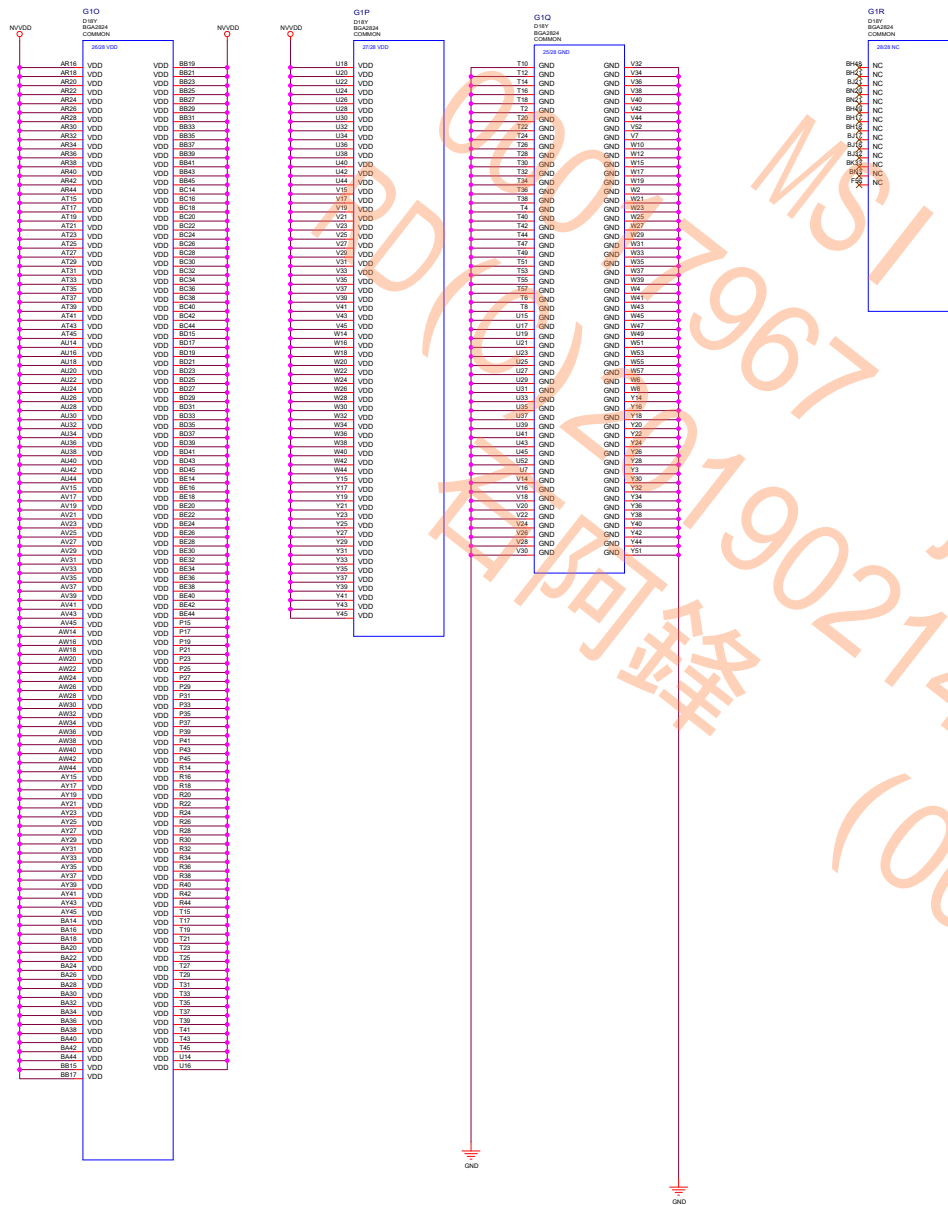


## GPU PWR and GND



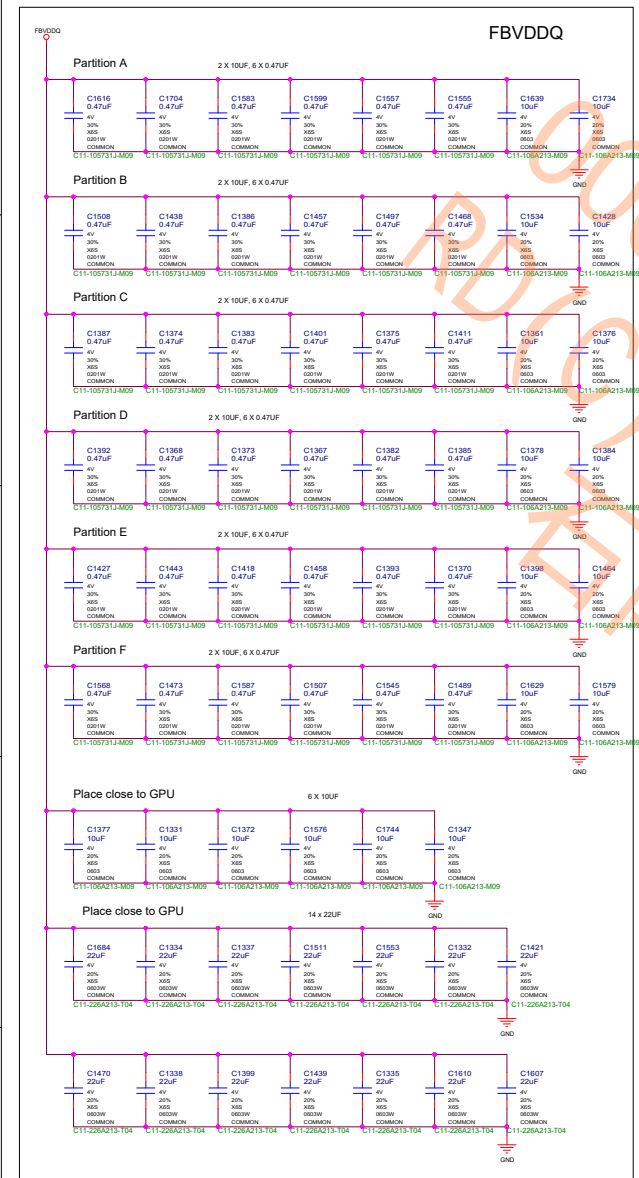


## GPU PWR GND NCs

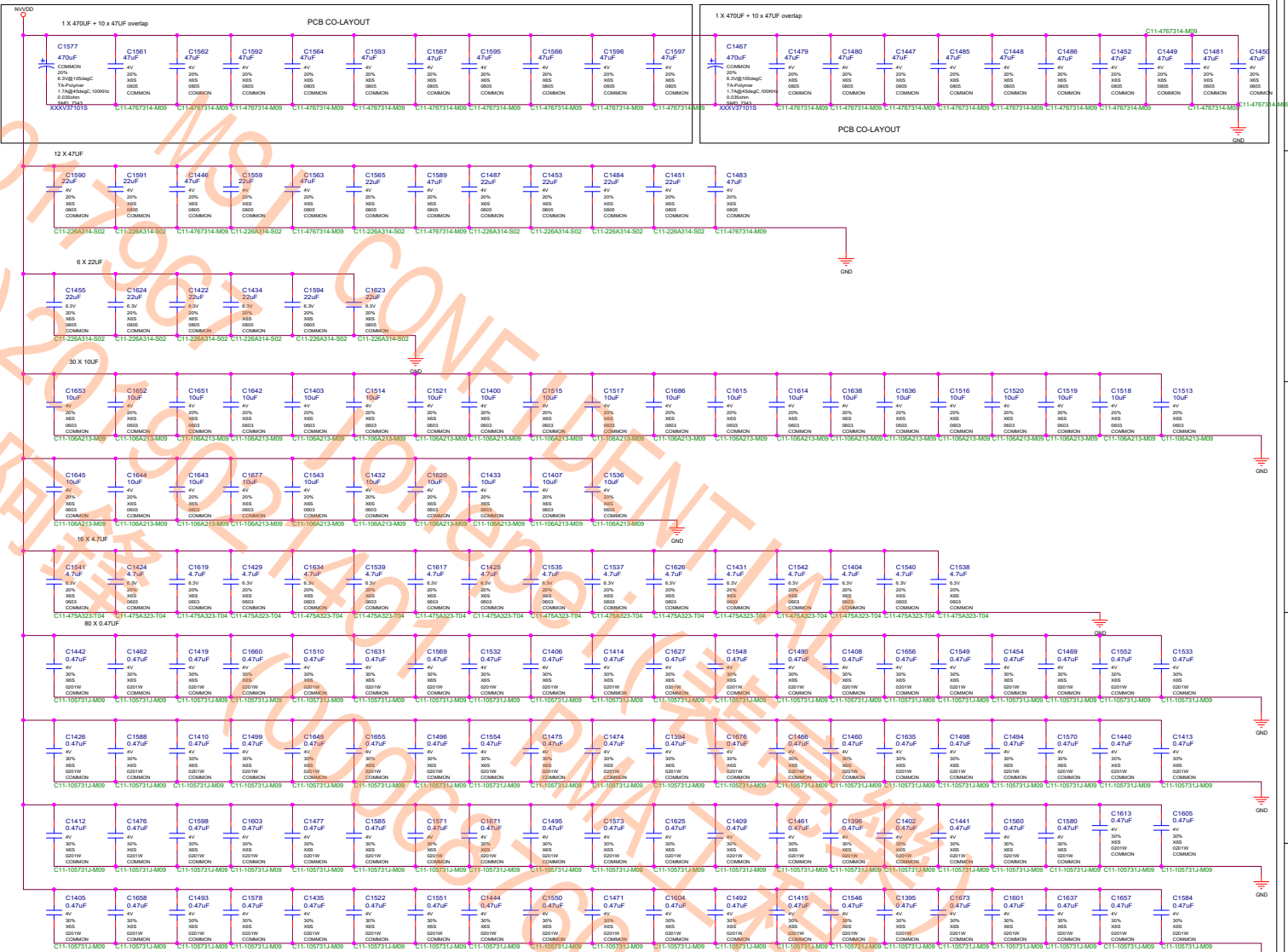




## GPU Decoupling



## NVVDD

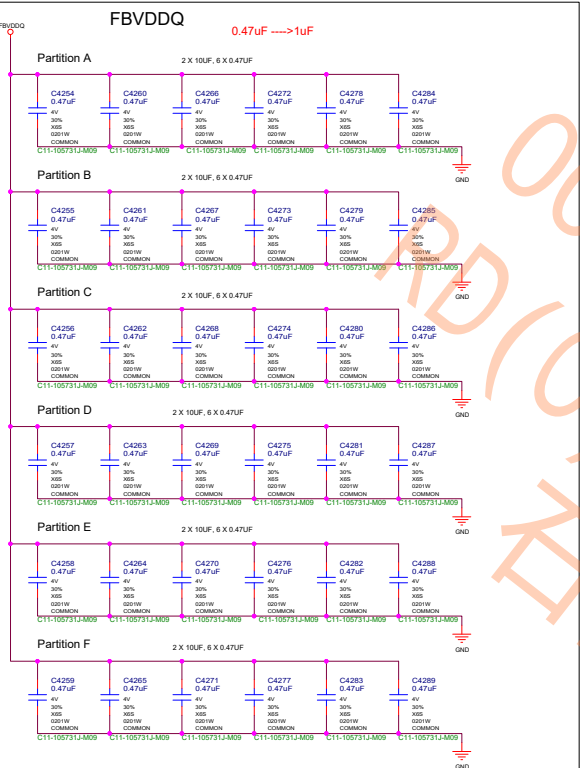


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Size: Custom  
Doc: Document Description  
Rev: 1.0  
Date: Thursday, August 23, 2018  
Sheet: 22 of 66

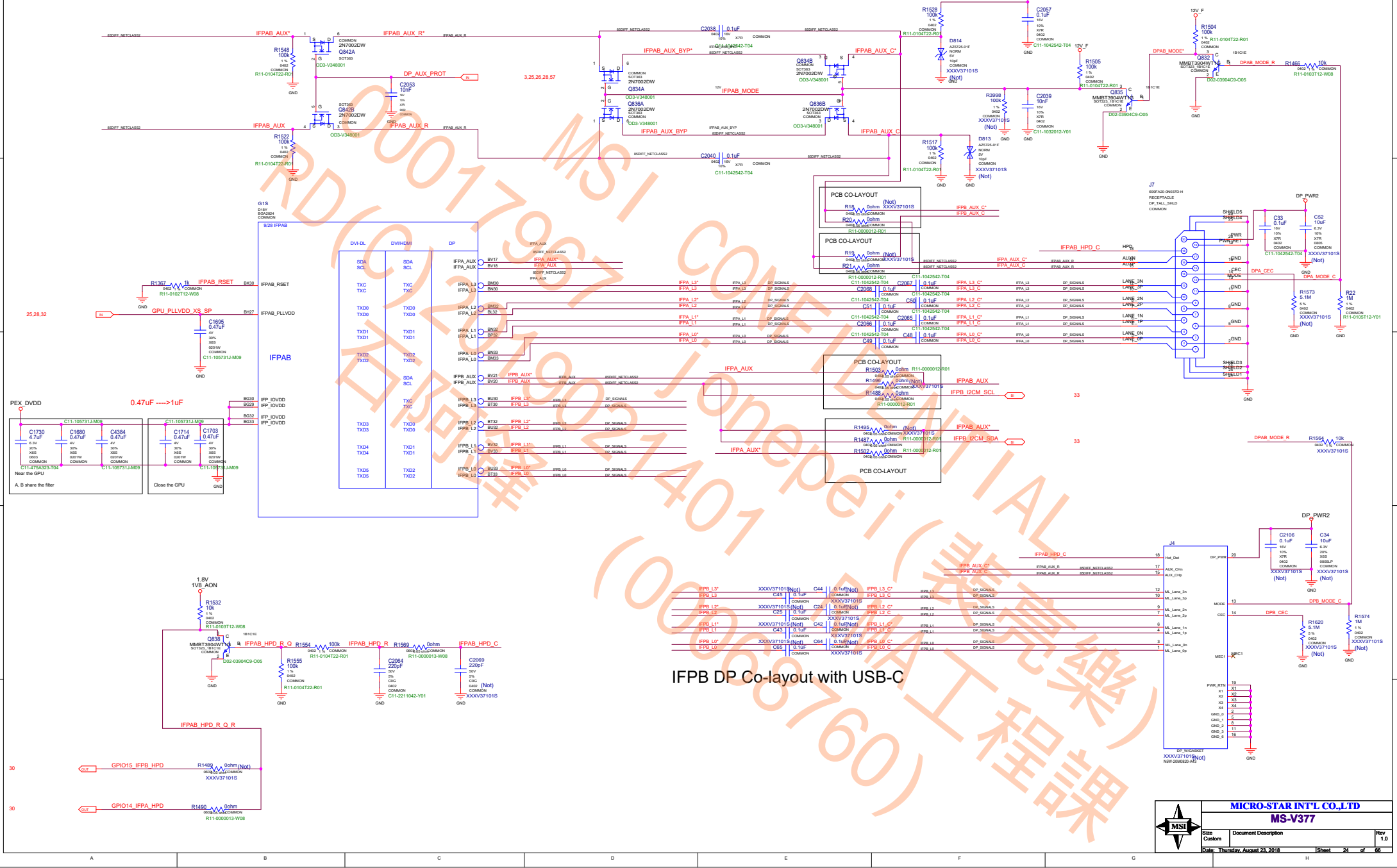


GPU Decoupling





## IFPAB TALL-DP





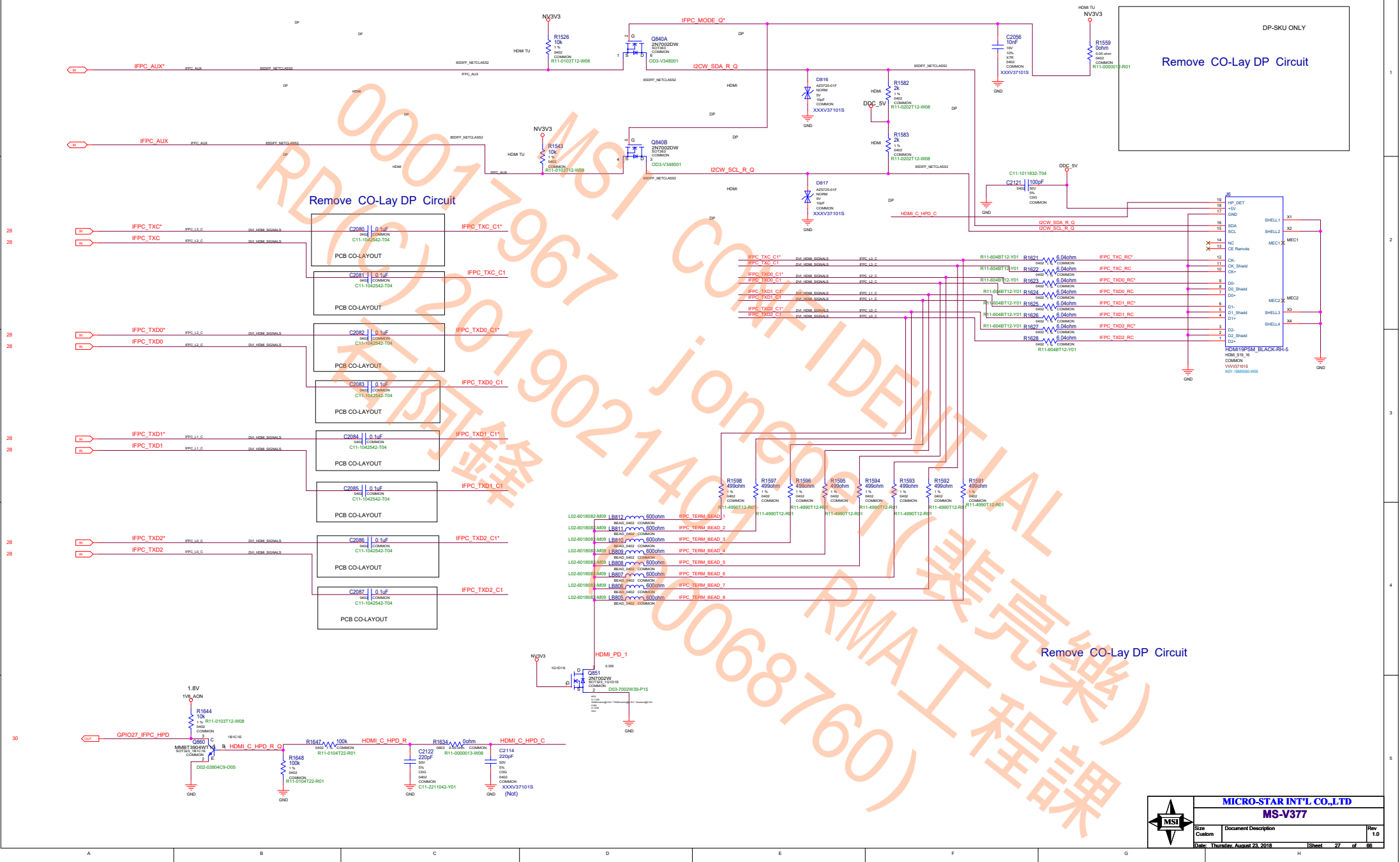




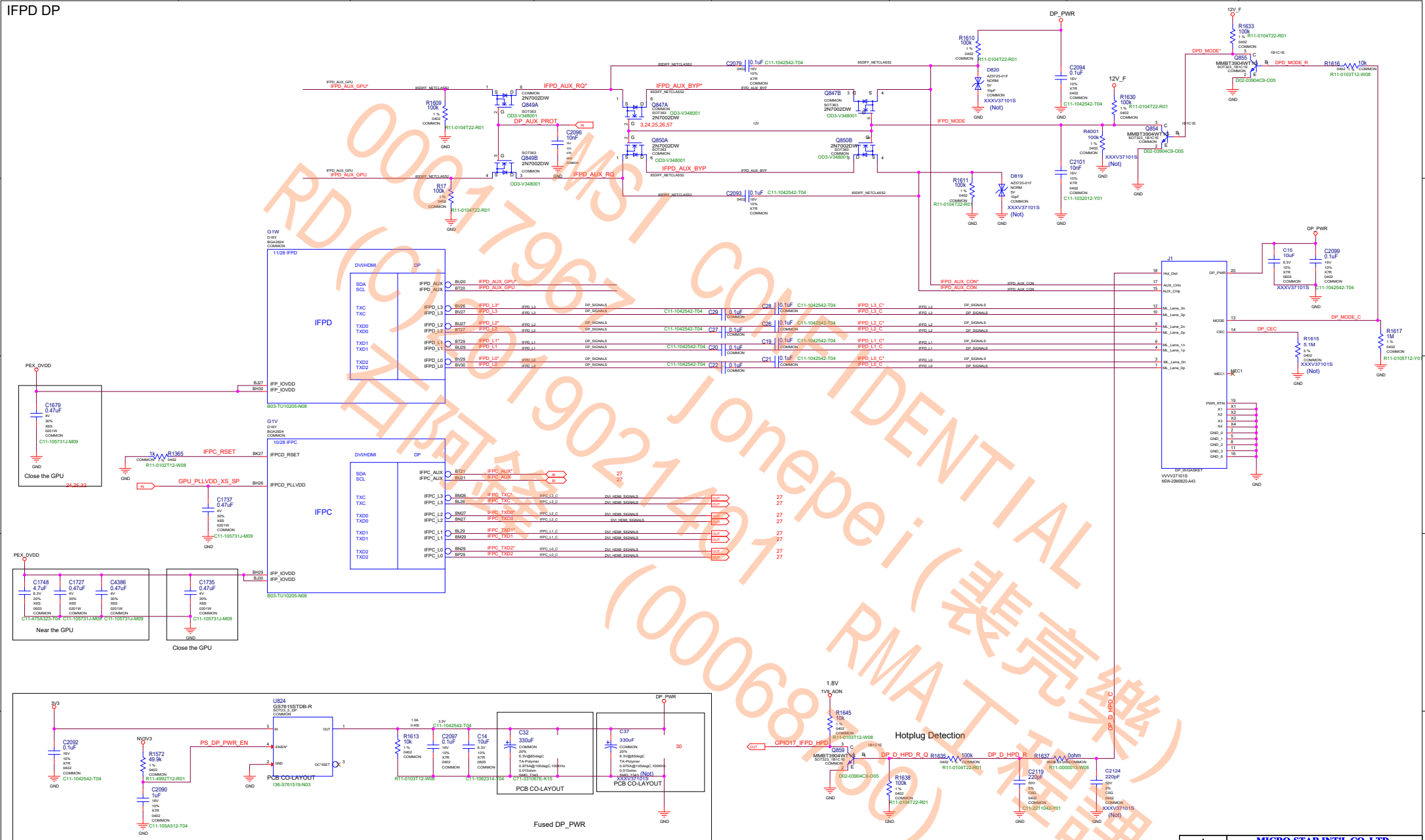




IFPC HDMI 2.0/DP









## NVHS Interface and FRAME LOCK

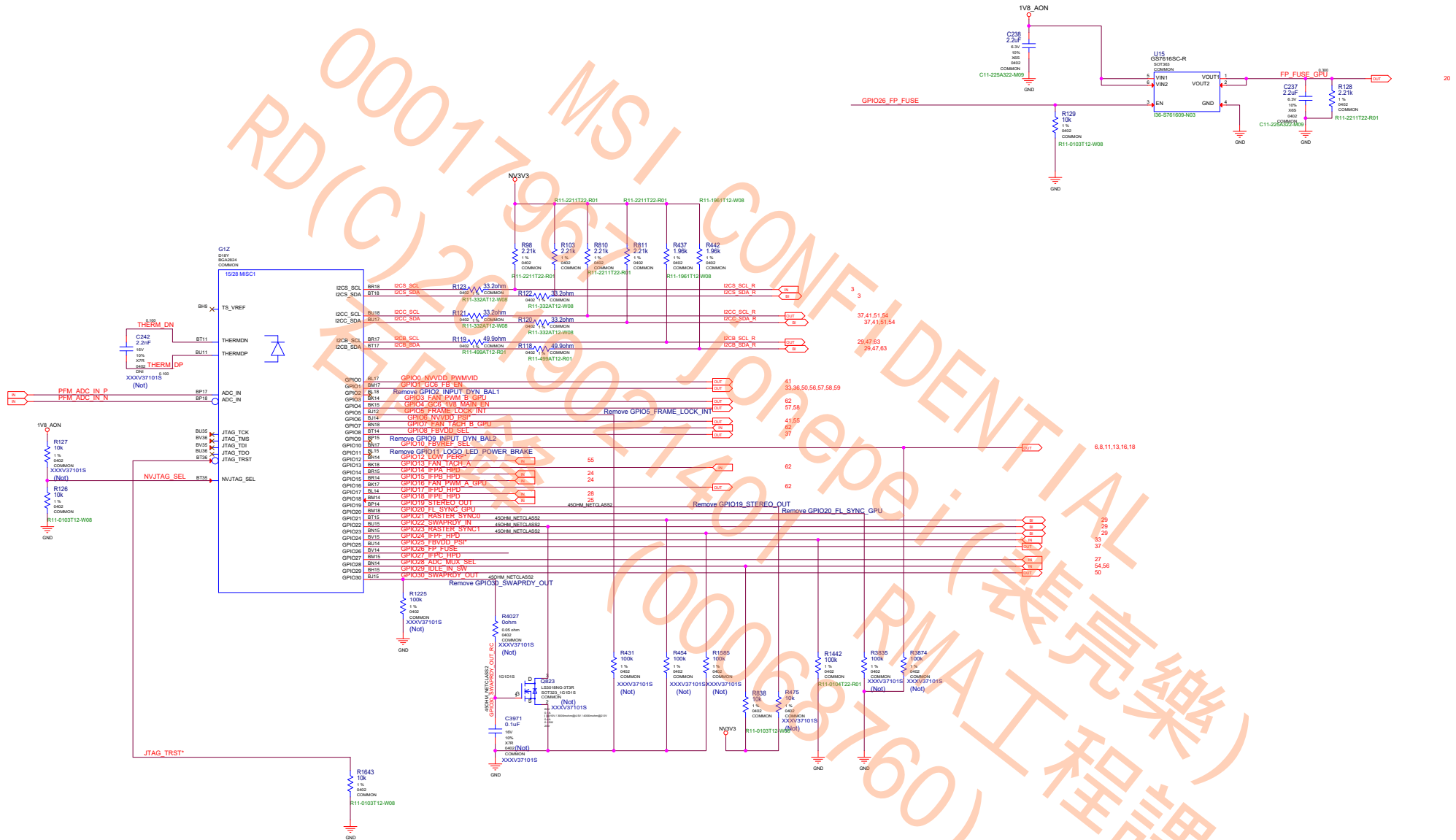


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**MS-V377**

Size Custom	Document Description	Rev 1.0
Date: Thursday, August 23, 2018	Sheet 29 of 66	



## MISC1: Fan, Thermal, JTAG, GPIO, STEREO





## MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

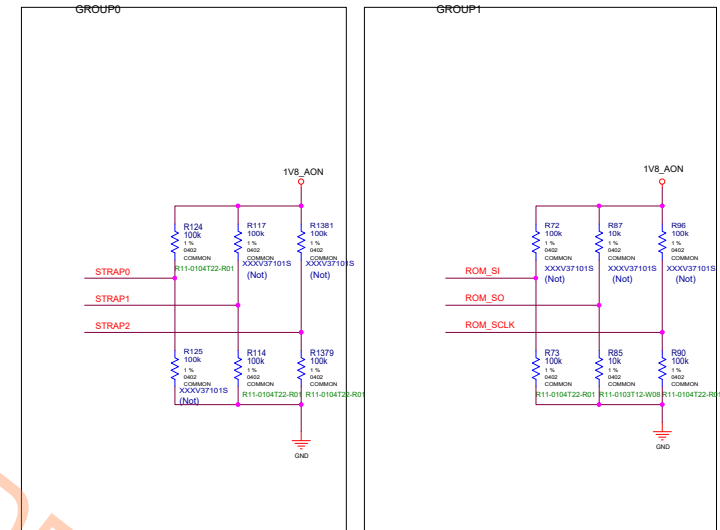
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCI_E_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

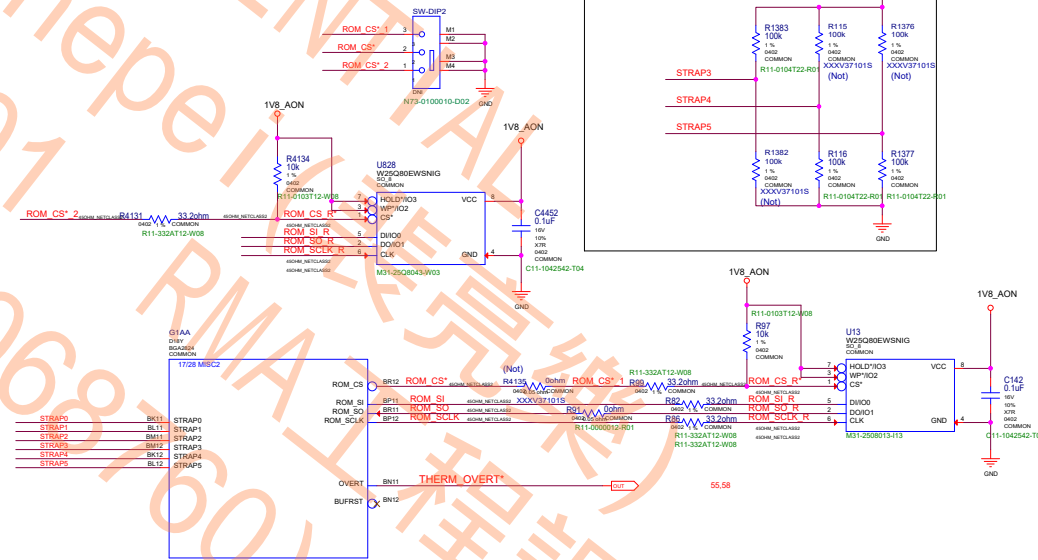
Default  
SKU 200

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGNAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

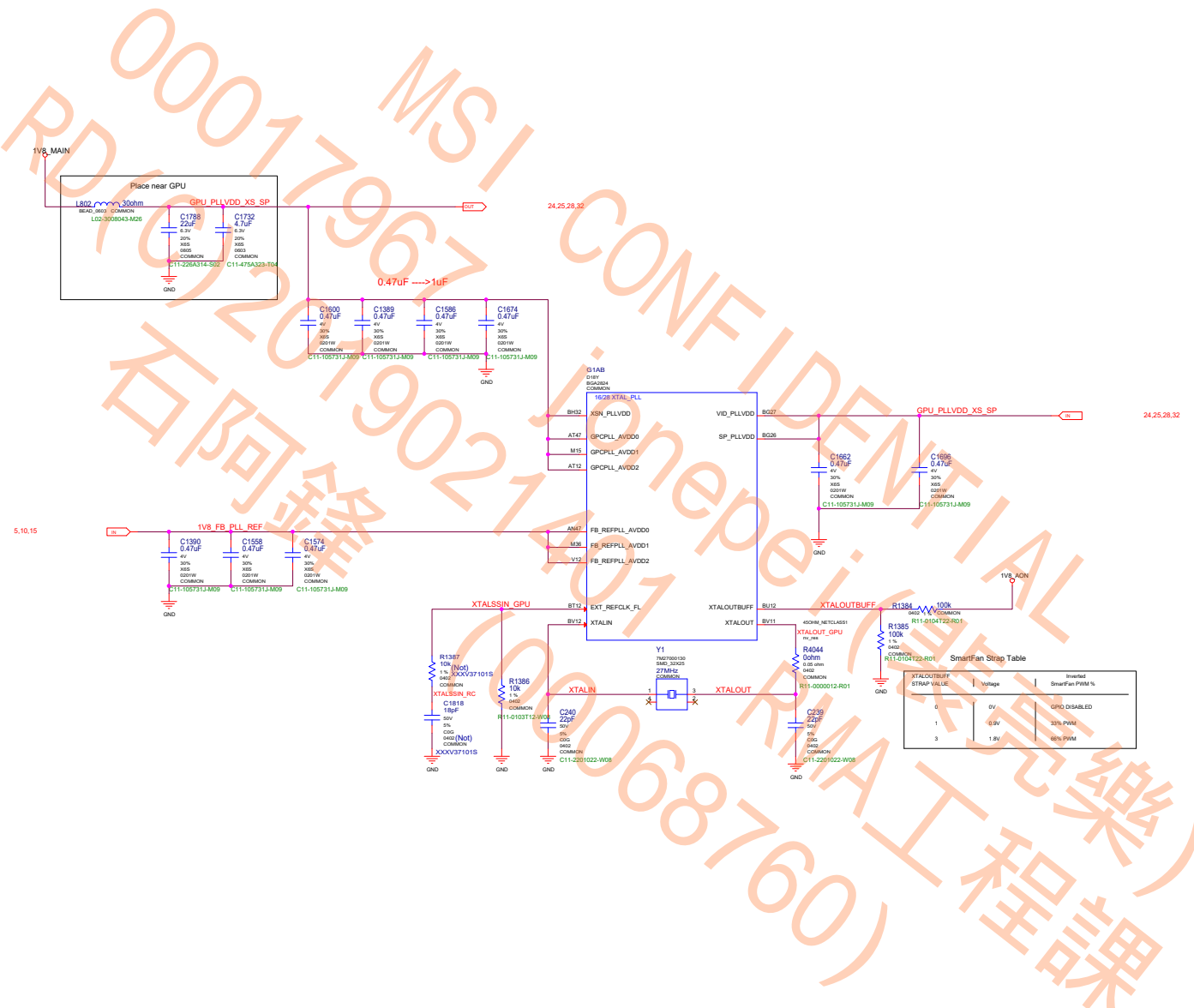
SKU 200



Add Dual BIOS

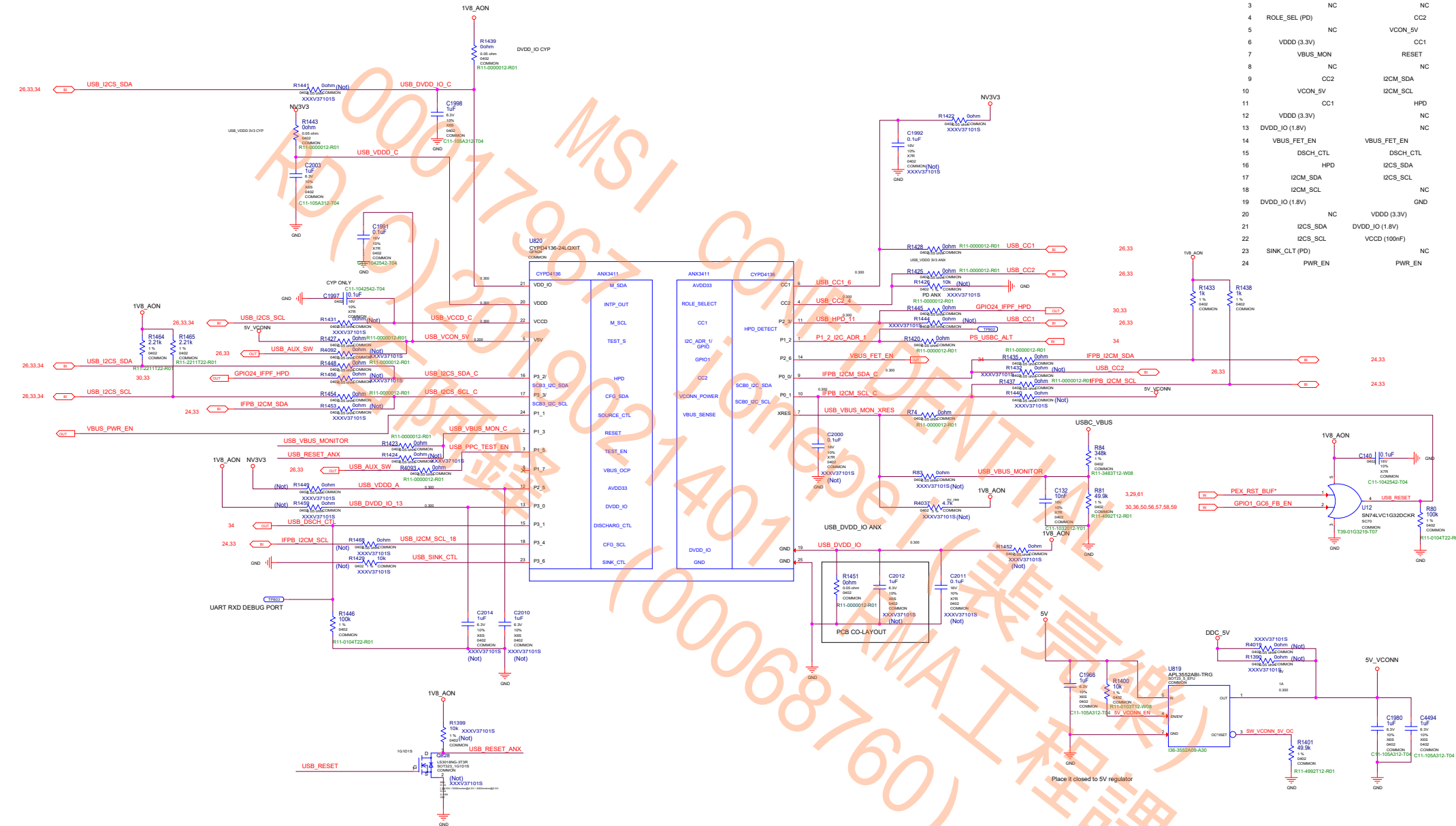








MISC: USB PPC



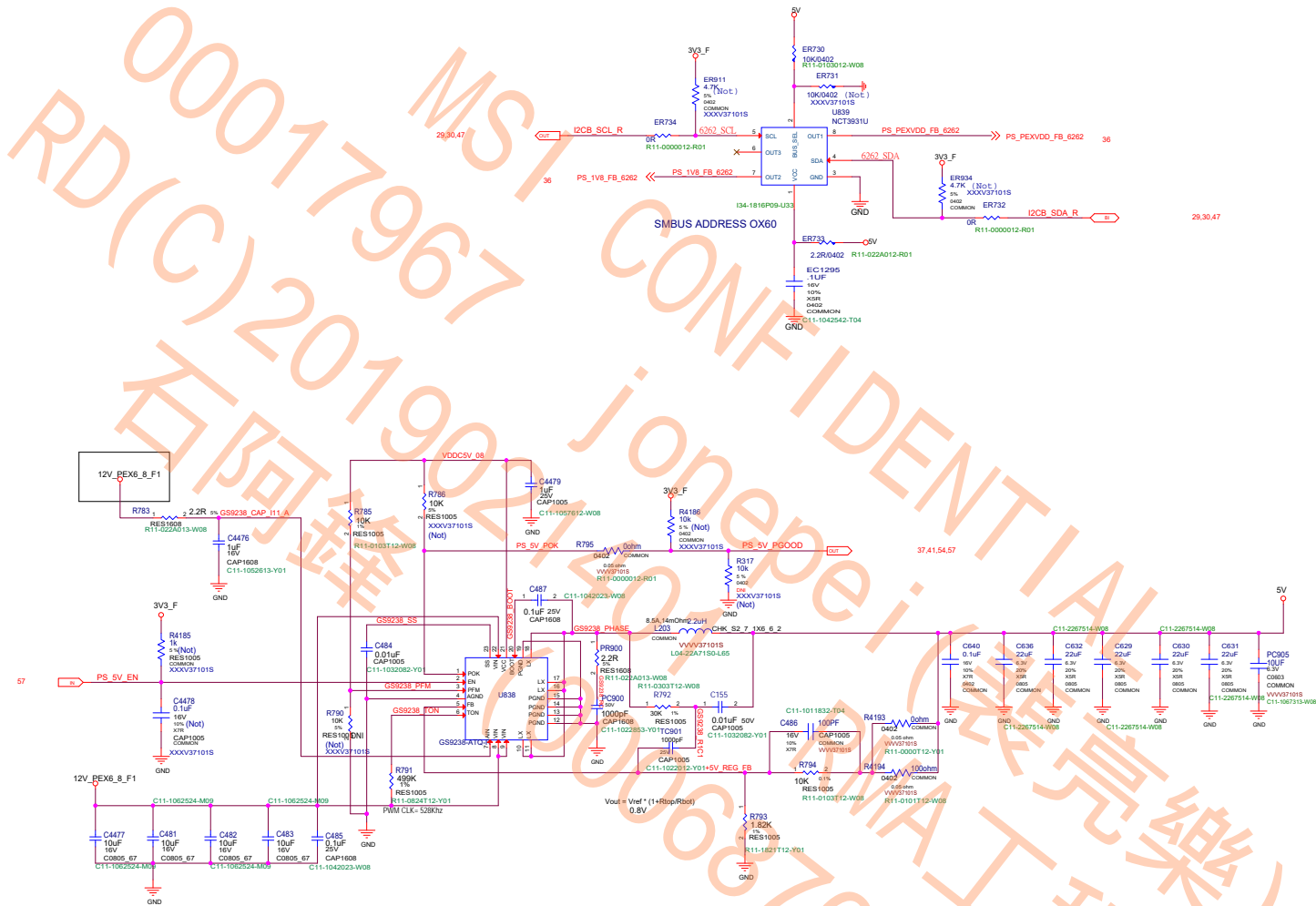
PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDO (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDO (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDO (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100F)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN







PS: 5V, 5V\_BACKUP

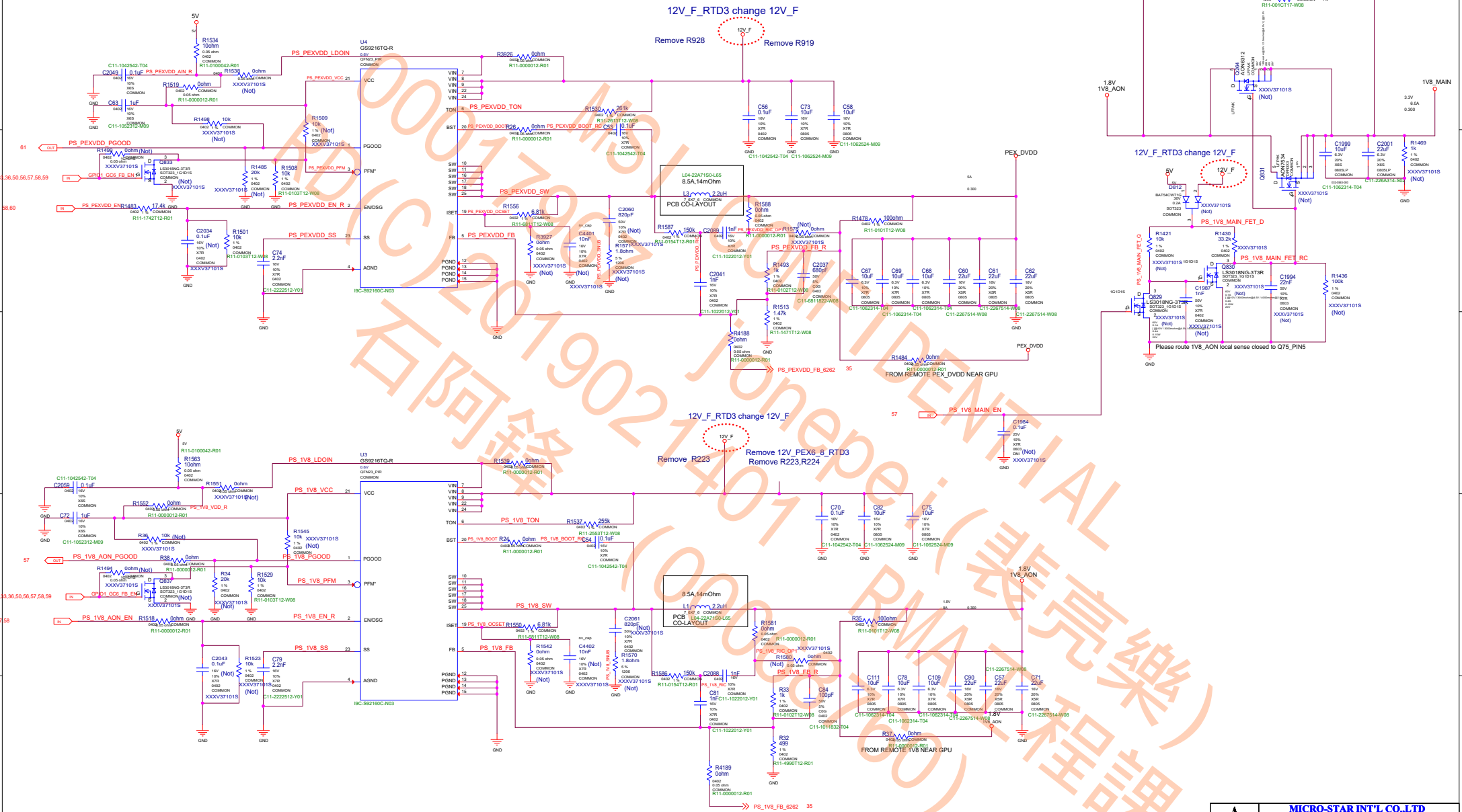


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MS-V377

Size Custom	Document Description <b>GPU Decoupling</b>	Rev 1.0
Date: Thursday, August 23, 2018	Sheet 35 of 66	







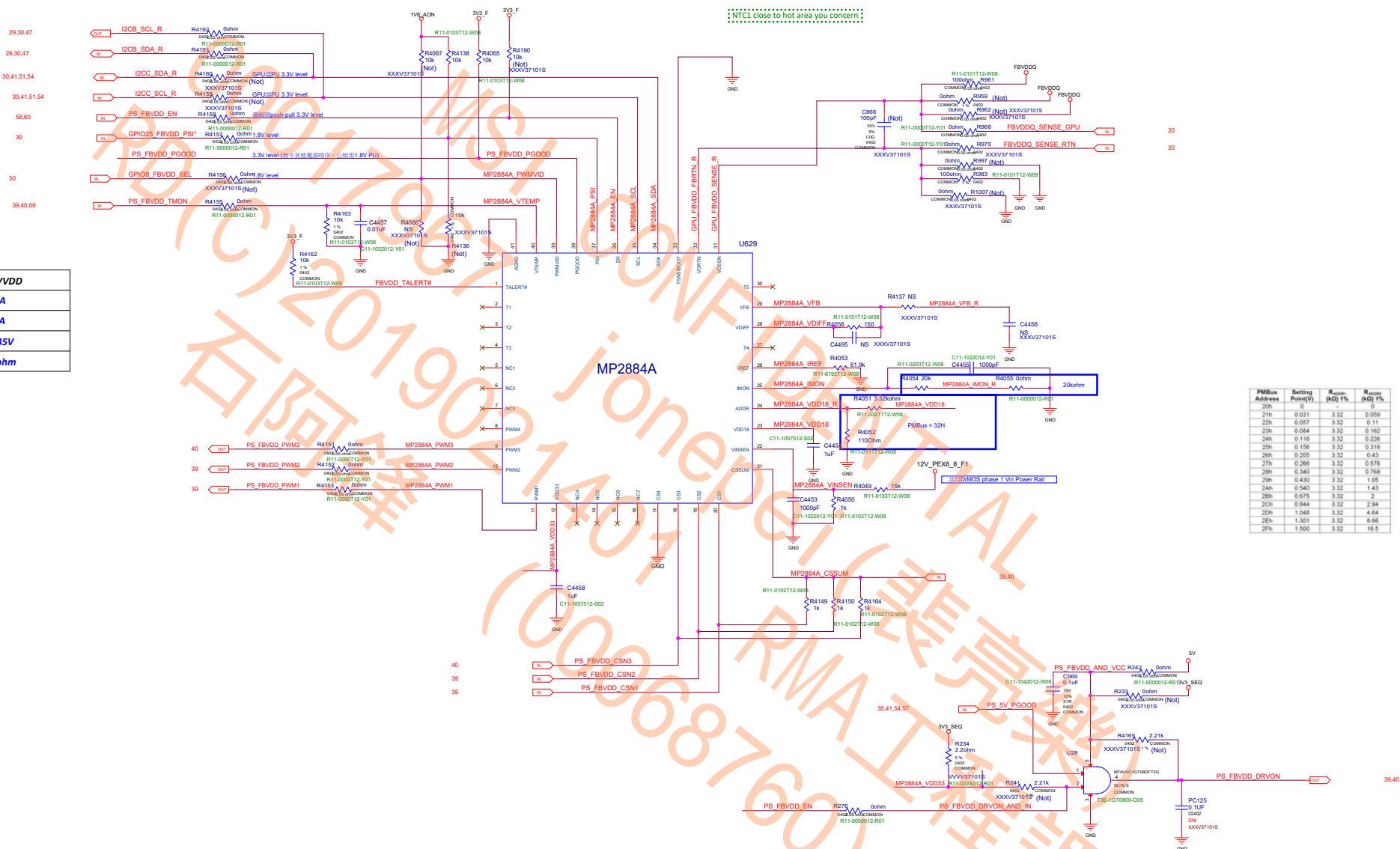
## PS: FBVDD Controller

EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

<b>PWMVID</b>	<b>Vout</b>
<i>High</i>	<i>VID in 24h</i>
<i>Hi-Z</i>	<i>VID in 21h</i>
<i>Low</i>	<i>VID in 1Fh</i>

	+NVVDD
TDC	??A
IccMax	??A
Vboot	1.35V
Load Line	0mohm



PMI#s Address	Setting Priority	Reason (pQI %)	Reason (pQI %)
20n	0	-	0
22n	0.031	3.2	0.059
22n	0.057	3.32	0.11
23n	0.084	3.32	0.162
24n	0.116	3.32	0.226
25n	0.156	3.32	0.316
26n	0.205	3.32	0.43
27n	0.266	3.32	0.576
28n	0.342	3.32	0.768
29n	0.430	3.32	1.05
2An	0.540	3.32	1.43
2Bn	0.675	3.32	2
2Cn	0.844	3.32	2.94
2Dn	1.048	3.32	4.64
2En	1.301	3.32	6.66
2Fn	1.604	3.32	8.68

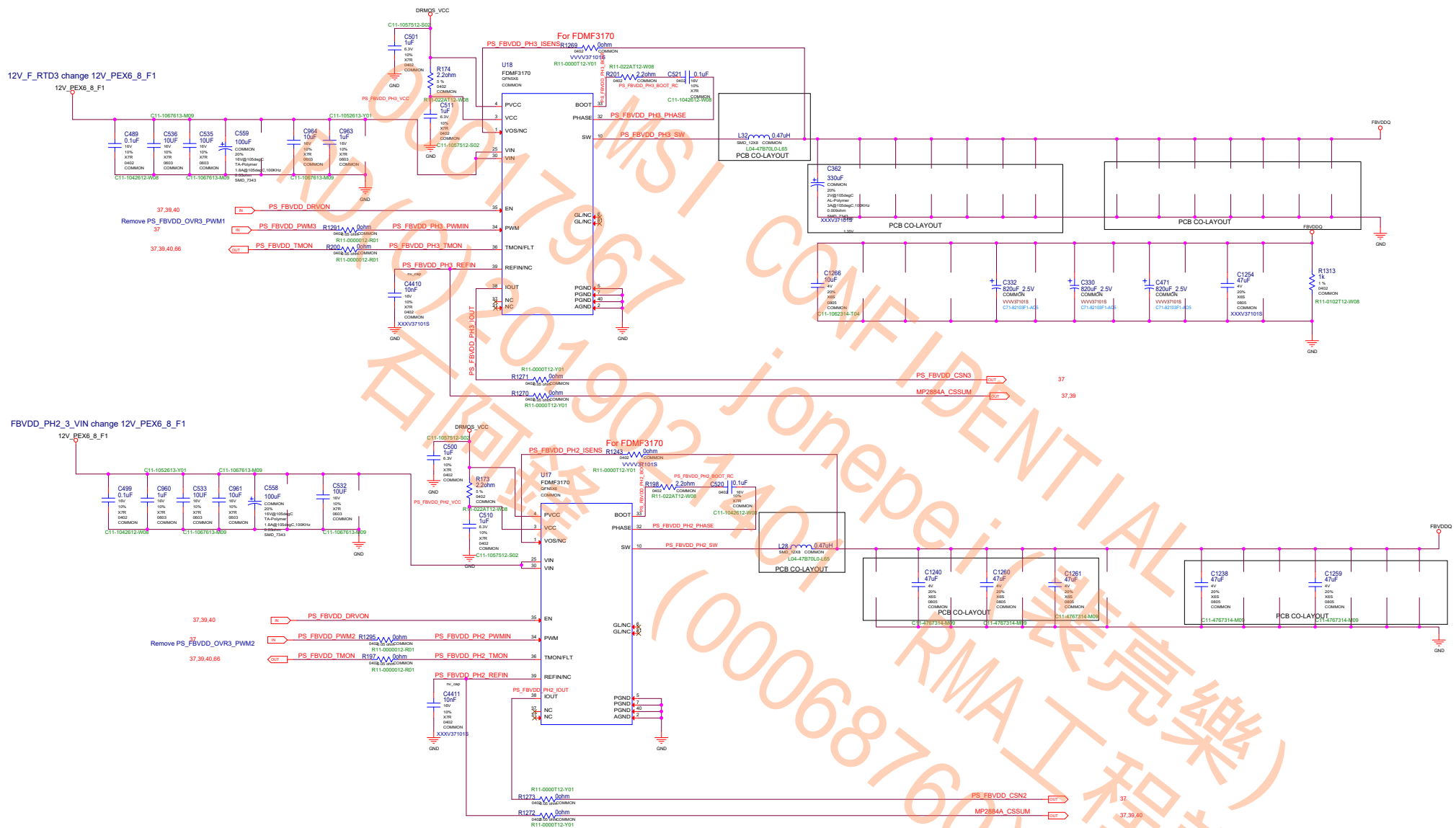




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RD(C)2019021401 RMA工程課  
石阿鋒 (00068760)



PS: FBVDD PH2,3

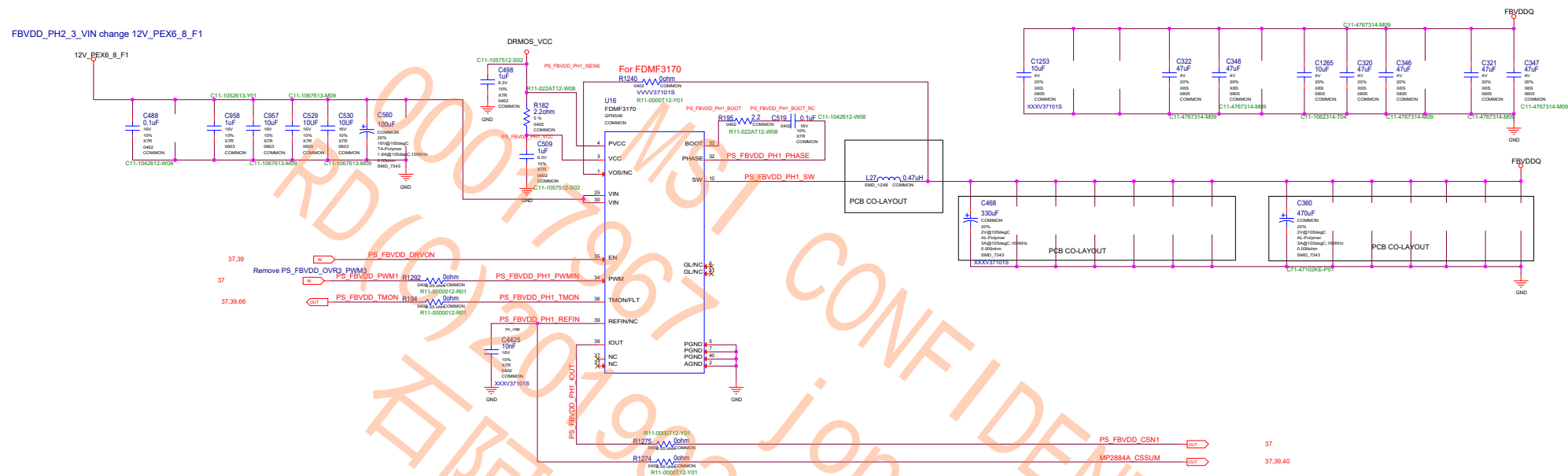


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MS-V377

Size Custom	Document Description	Rev 1.0
Date: Thursday, August 23, 2018		Sheet 39 of 66





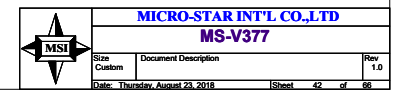
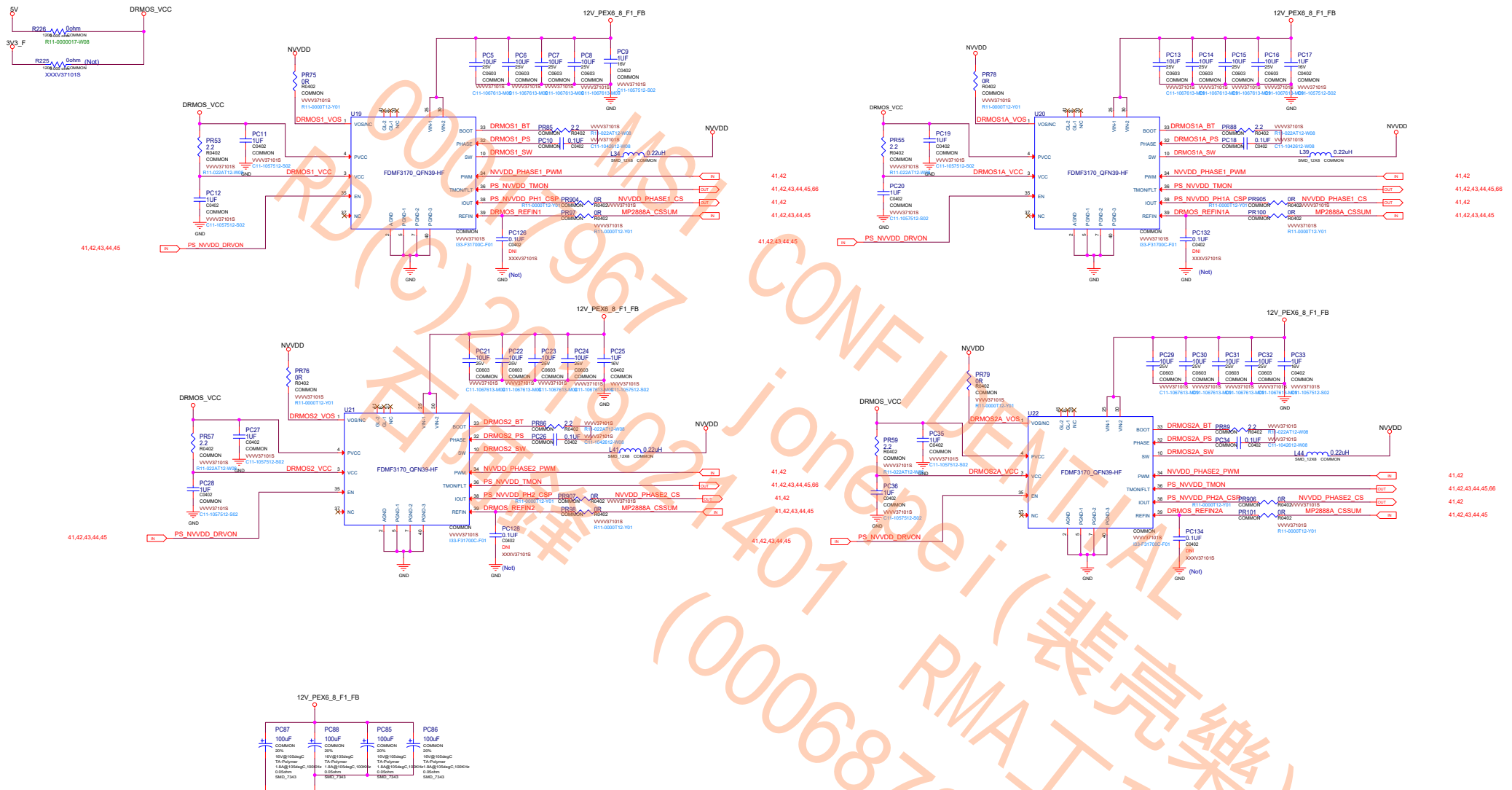
Remove 12V\_PEX\_FB ---->FBVDD\_PH2\_3\_VIN circuit



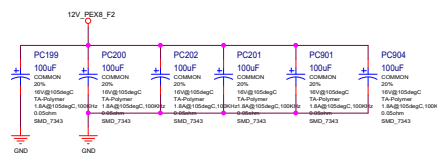
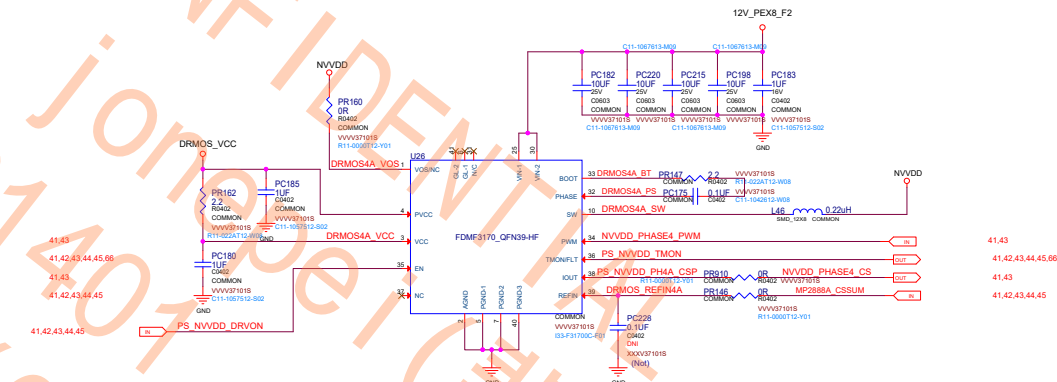
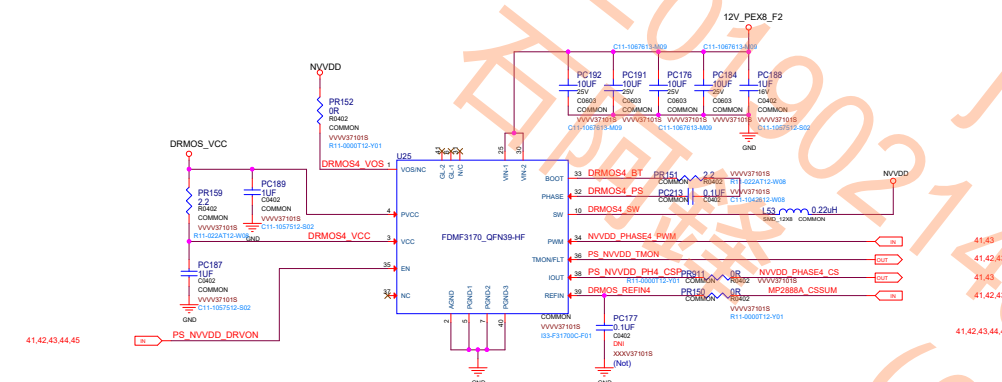
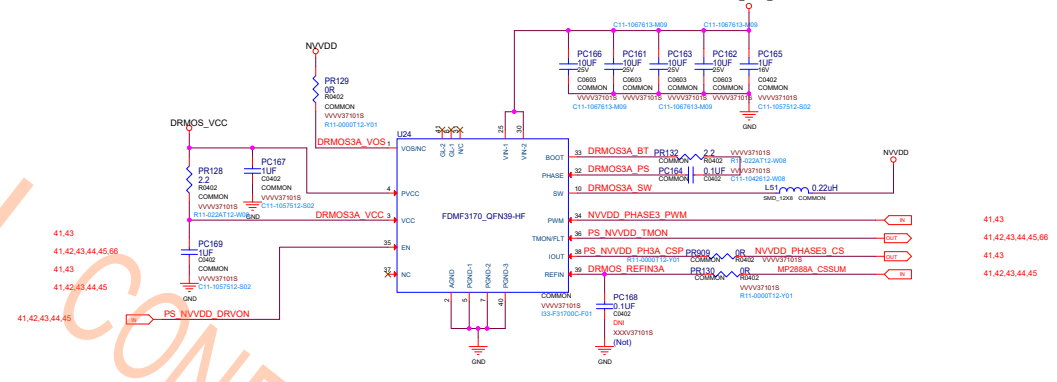
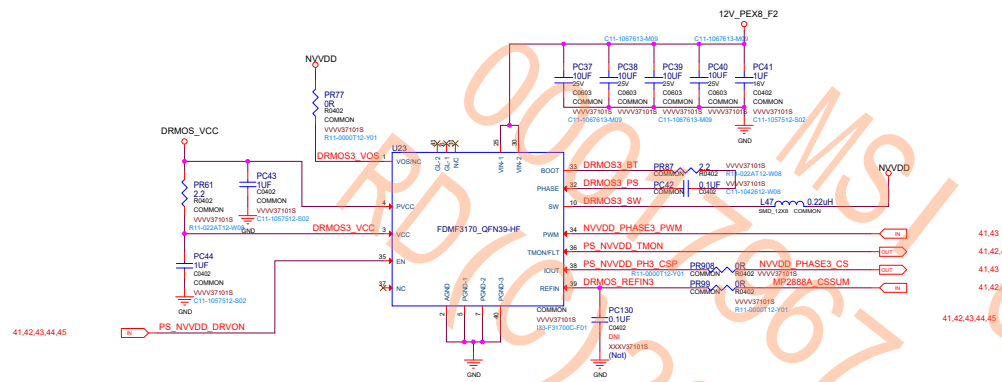




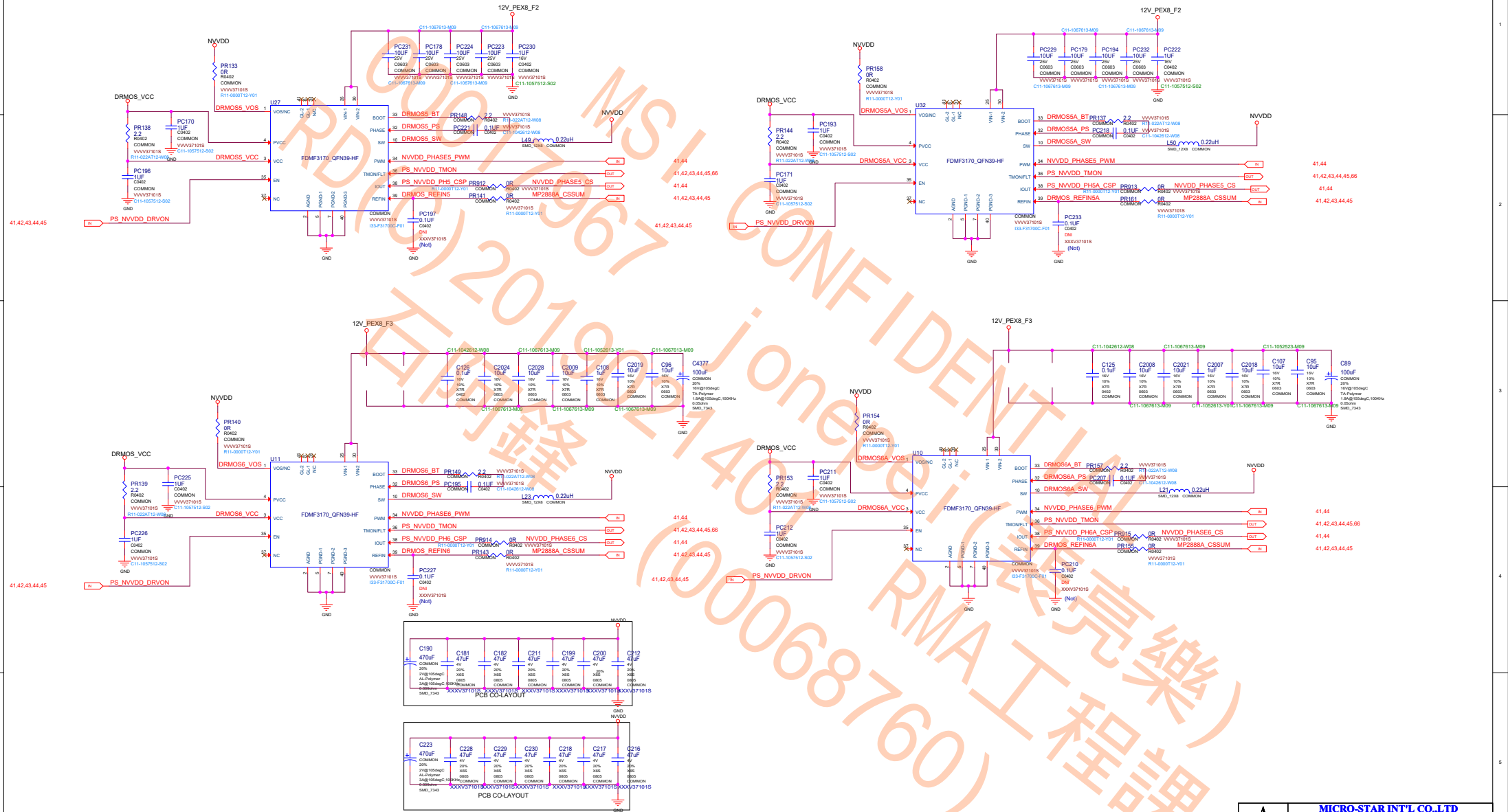
## PS: NVVDD Phase 1~4









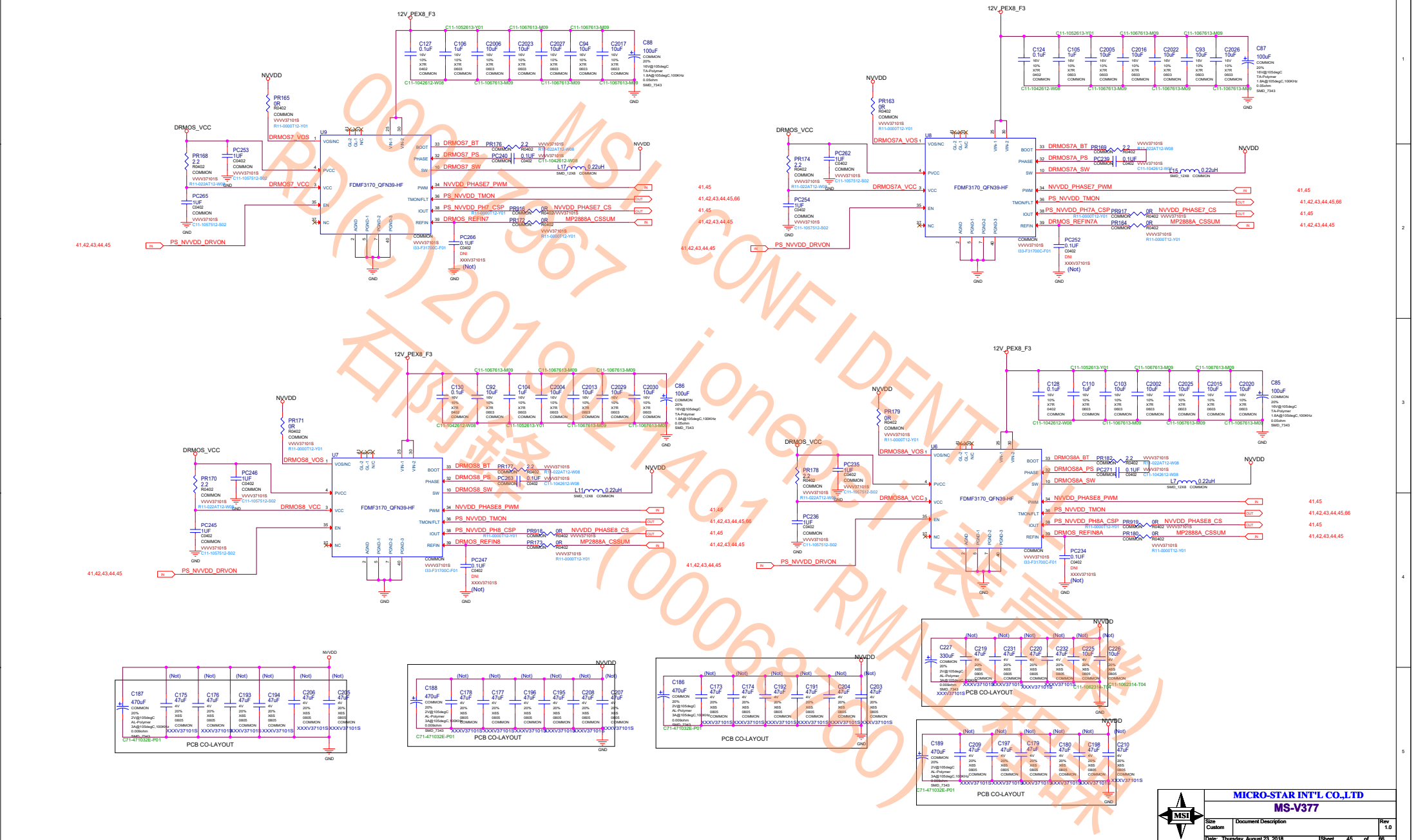


MICRO-STAR INT'L CO., LTD  
MS-V377

Size	Document Description	Rev
Custom		1.0

Date: Thursday, August 23, 2018 Sheet 44 of 66









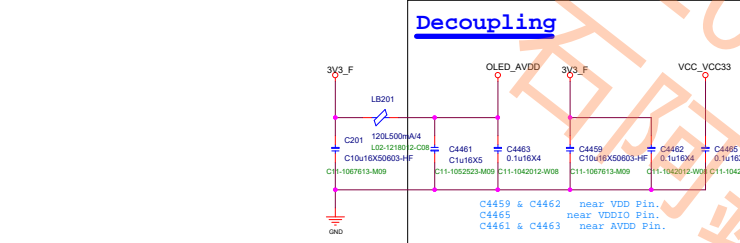
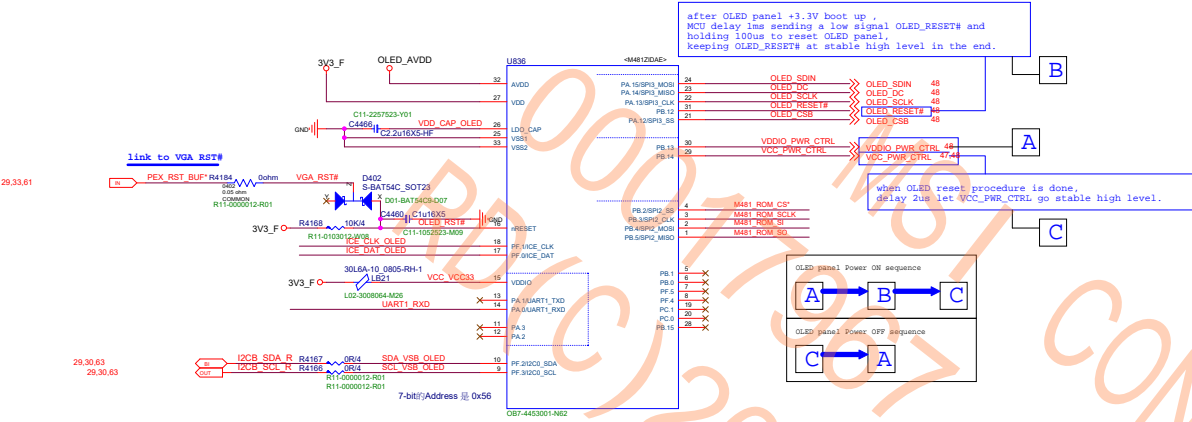
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MS-V377

Size Custom	Document Description <b>PS: NVDD - MP2888A</b>	Rev 1.0
Date: Thursday, August 23, 2018		Sheet 46 of 66

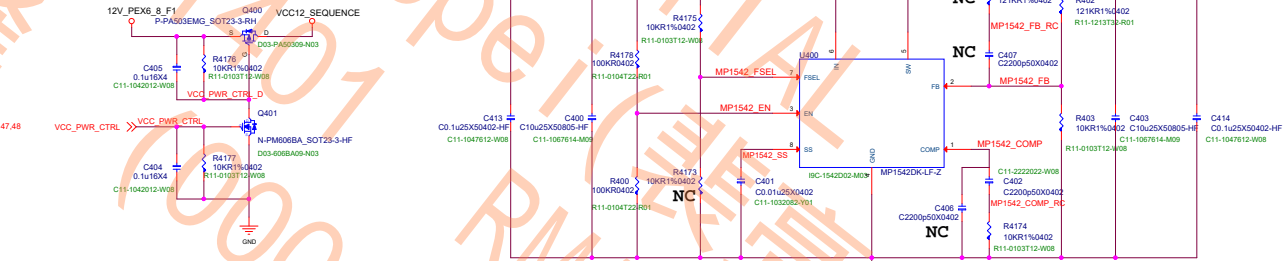


PS: NVDD PH 9,10  
32 PIN OLED MCU



MPS1542 BUCK BOOST FOR OLED POWER 12Vin 16.5Vout

+16.5V power up sequence



PIN FUNCTIONS

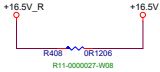
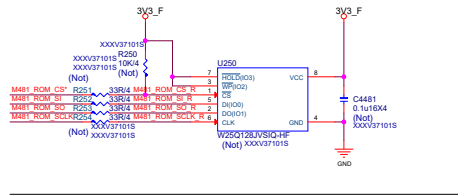
Pin #	Name	Description
1	COMP	Compensation Pin. Connect a capacitor and resistor in series to ground for loop stability.
2	FB	Feedback Input. Reference voltage is 1.25V. Connect a resistor divider to this pin.
3	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input source (through a 100kΩ pull-up resistor if $V_{IN} > 6V$ ) for automatic startup. EN cannot be left floating.

I2C and UART Reserve

FW update



External 3.3V SPI ROM, 128M(16Mx8bit)






[illegible]



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石阿鋒 (00068760)

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	MS-V377		
	Size	Document Description	Rev
	Custom		1.0
Date: Tuesday, August 21, 2018		Sheet 49 of 68	



PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

Remove 12V\_F\_RTD3 circuit

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

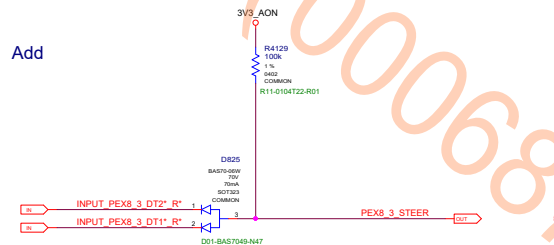
Remove 3V3\_RTD3 circuit







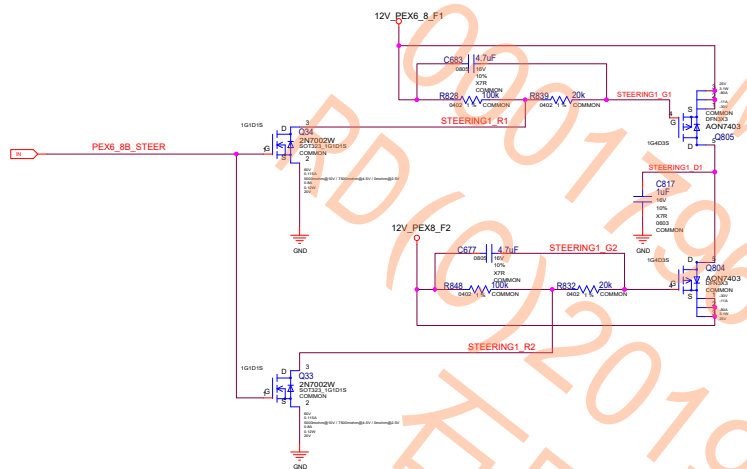




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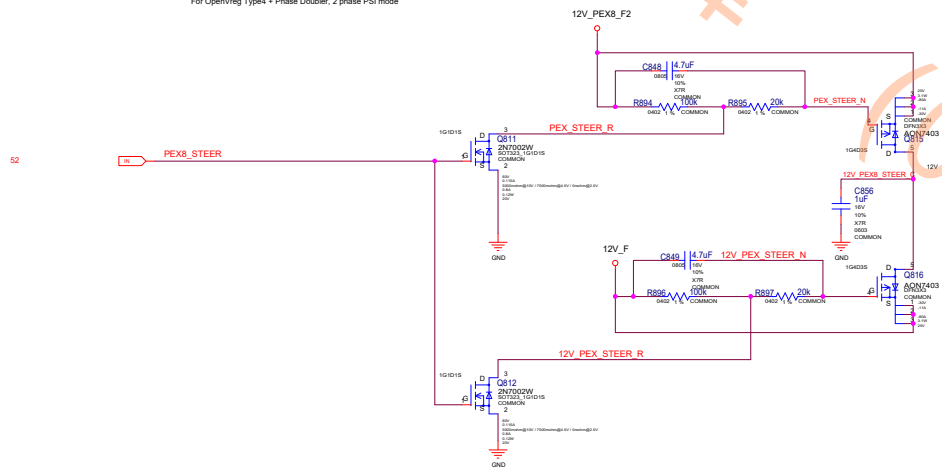


12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

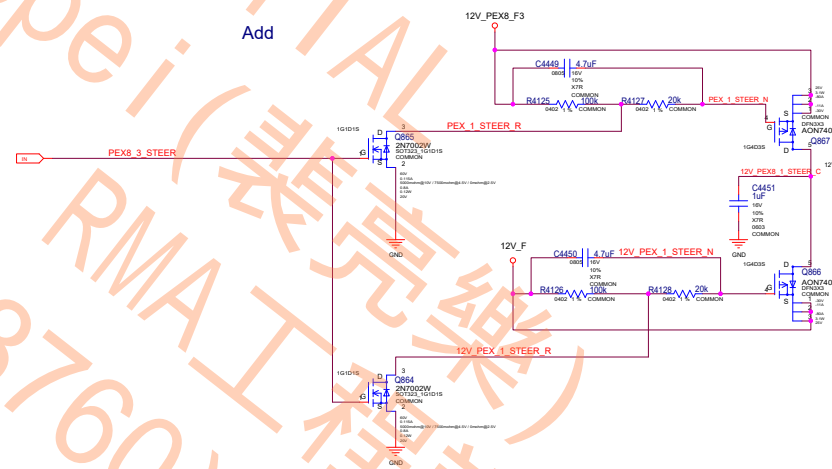


12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVing Type4 + Phase Doubler, 2 phase PSI mode

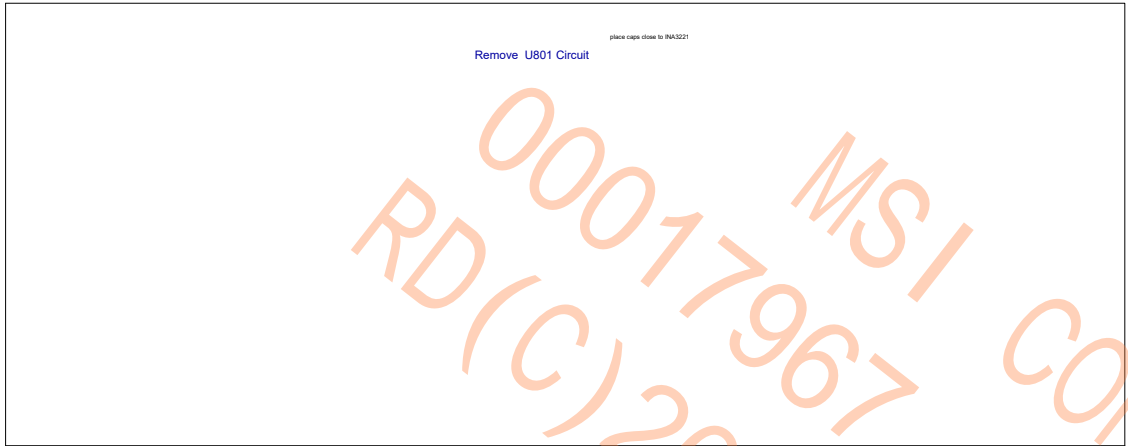


Add

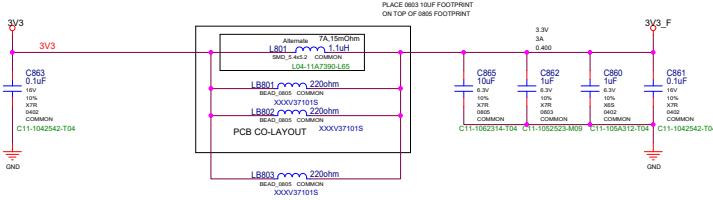




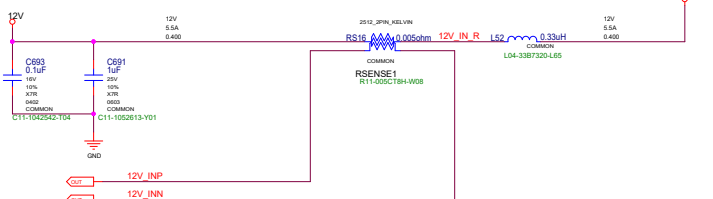
PS: Inputs, Filtering, and Monitoring



PEX 3V3 INPUT - 10W

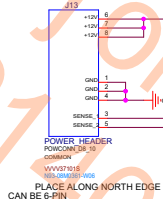
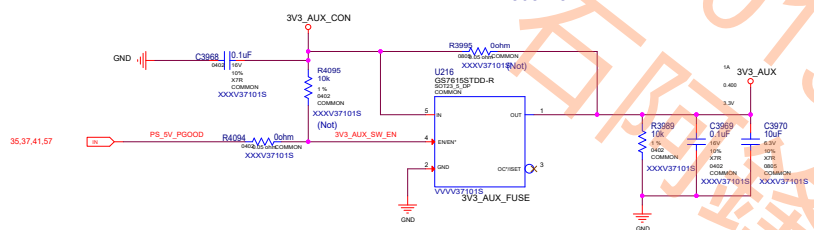


PEX 12V INPUT - 66W

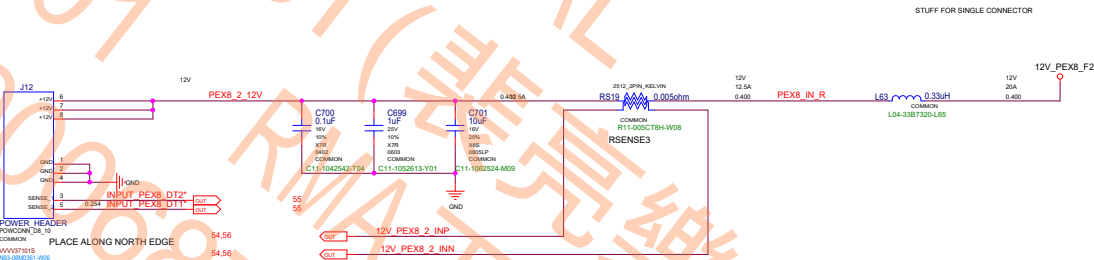


Remove R808 R812

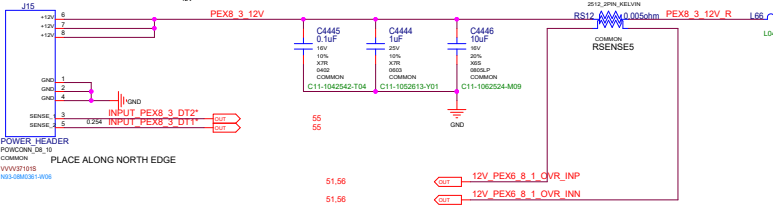
PEX6 INPUT 1 - 2x3 PCIe CON 75W



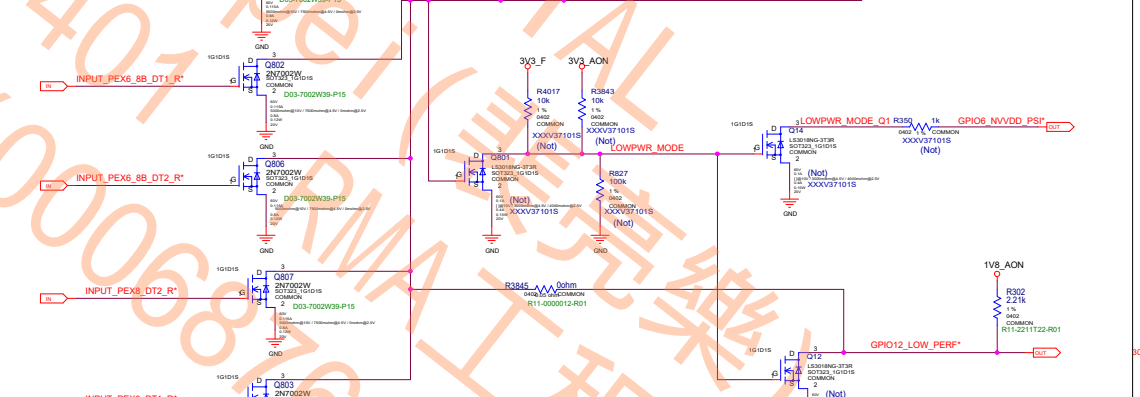
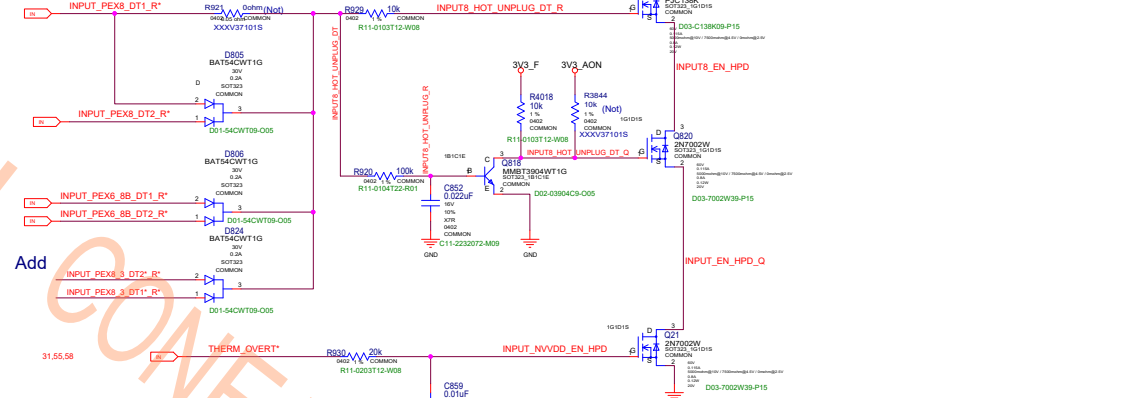
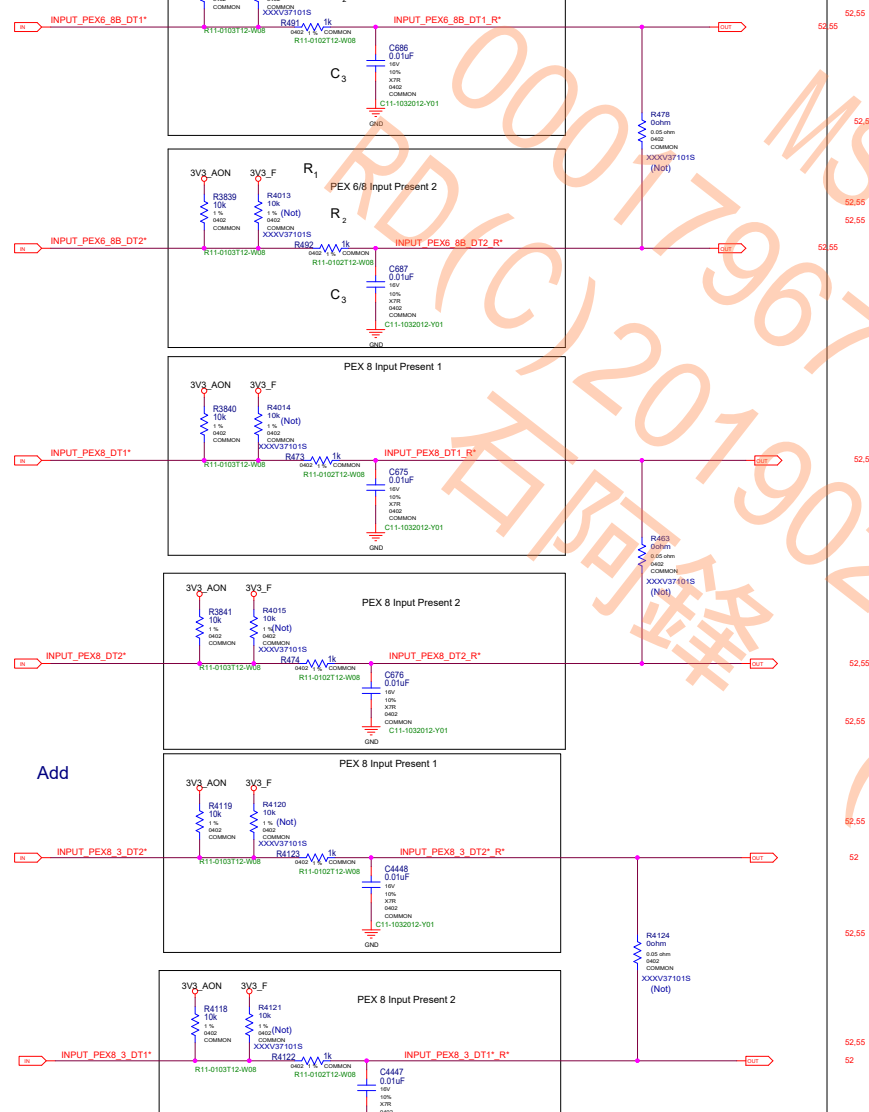
PEX8 INPUT 2 - 2x4 PCIe CON 150W



Add









## PS: Pre-Filter

STUFF IF USING 2XMUX

R11-000012-R01

R826 100k

R825 100k

R824 100k

R823 100k

R822 100k

R821 100k

R820 100k

R819 100k

R818 100k

R817 100k

R816 100k

R815 100k

R814 100k

R813 100k

R812 100k

R811 100k

R810 100k

R809 100k

R808 100k

R807 100k

R806 100k

R805 100k

R804 100k

R803 100k

R802 100k

R801 100k

R800 100k

R799 100k

R798 100k

R797 100k

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R795 100k

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R767 100k

R766 100k

R765 100k

R764 100k

R763 100k

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R758 100k

R757 100k

R756 100k

R755 100k

R754 100k

R753 100k

R752 100k

R751 100k

R750 100k

R749 100k

R748 100k

R747 100k

R746 100k

R745 100k

R744 100k

R743 100k

R742 100k

R741 100k

R740 100k

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R733 100k

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R731 100k

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R516 100k

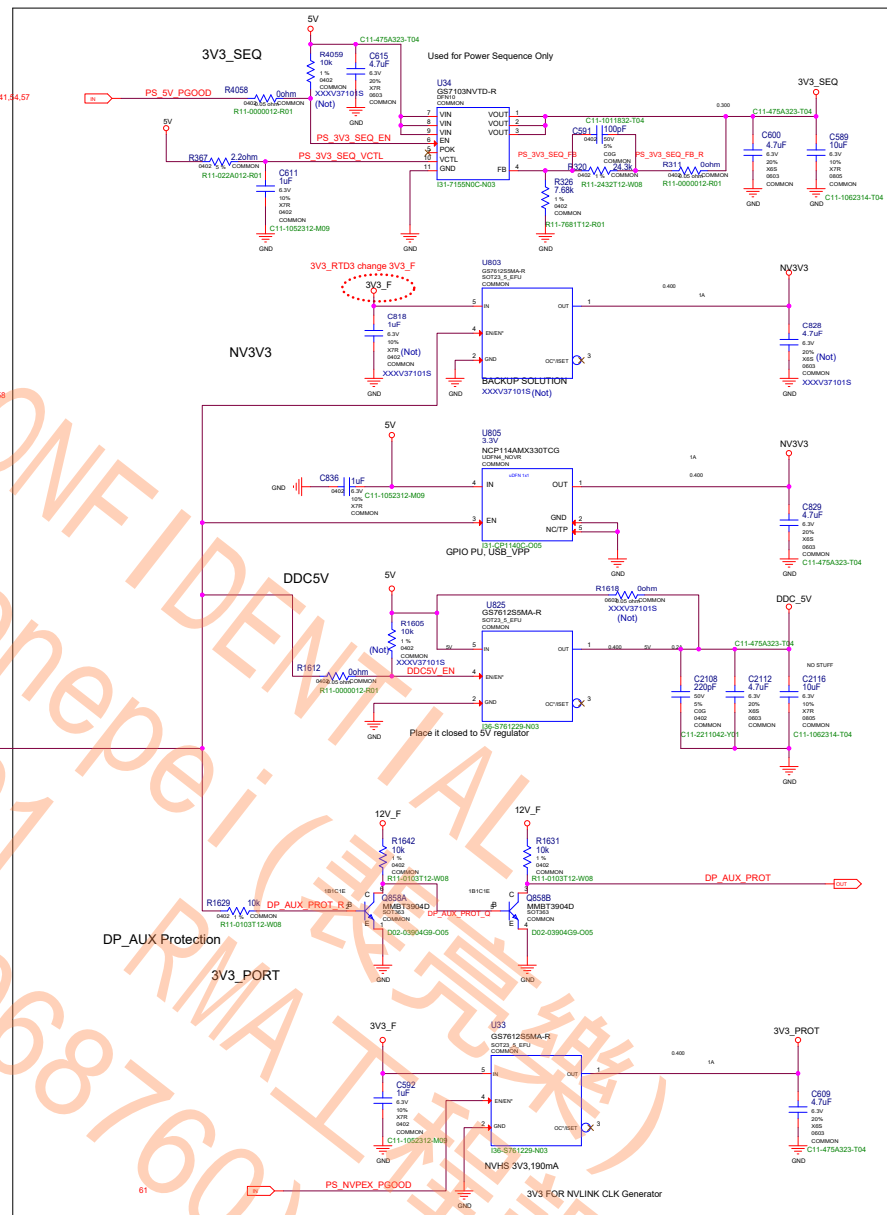
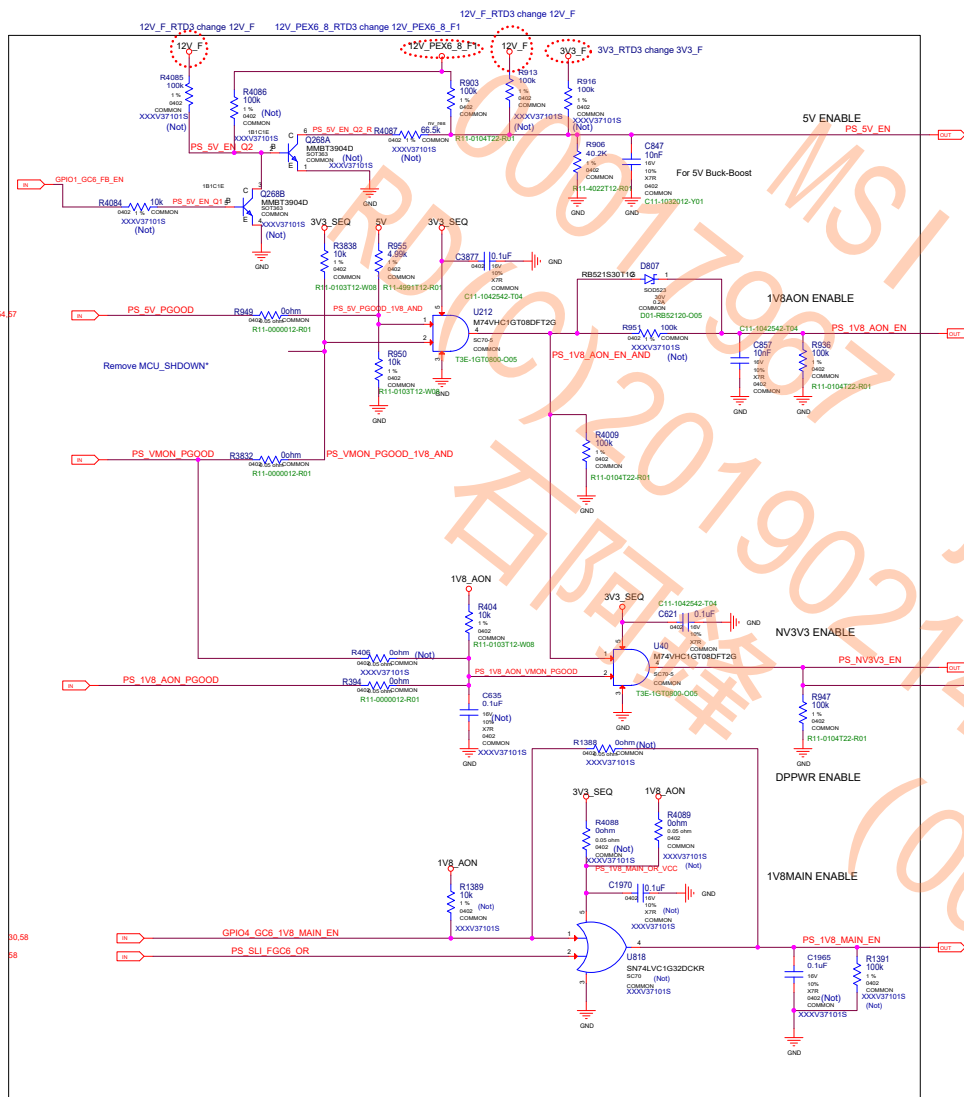
R515 100k

R514 100k

R513 100k



SEQUENCE:5V,1V8,NV3V3 ENABLE



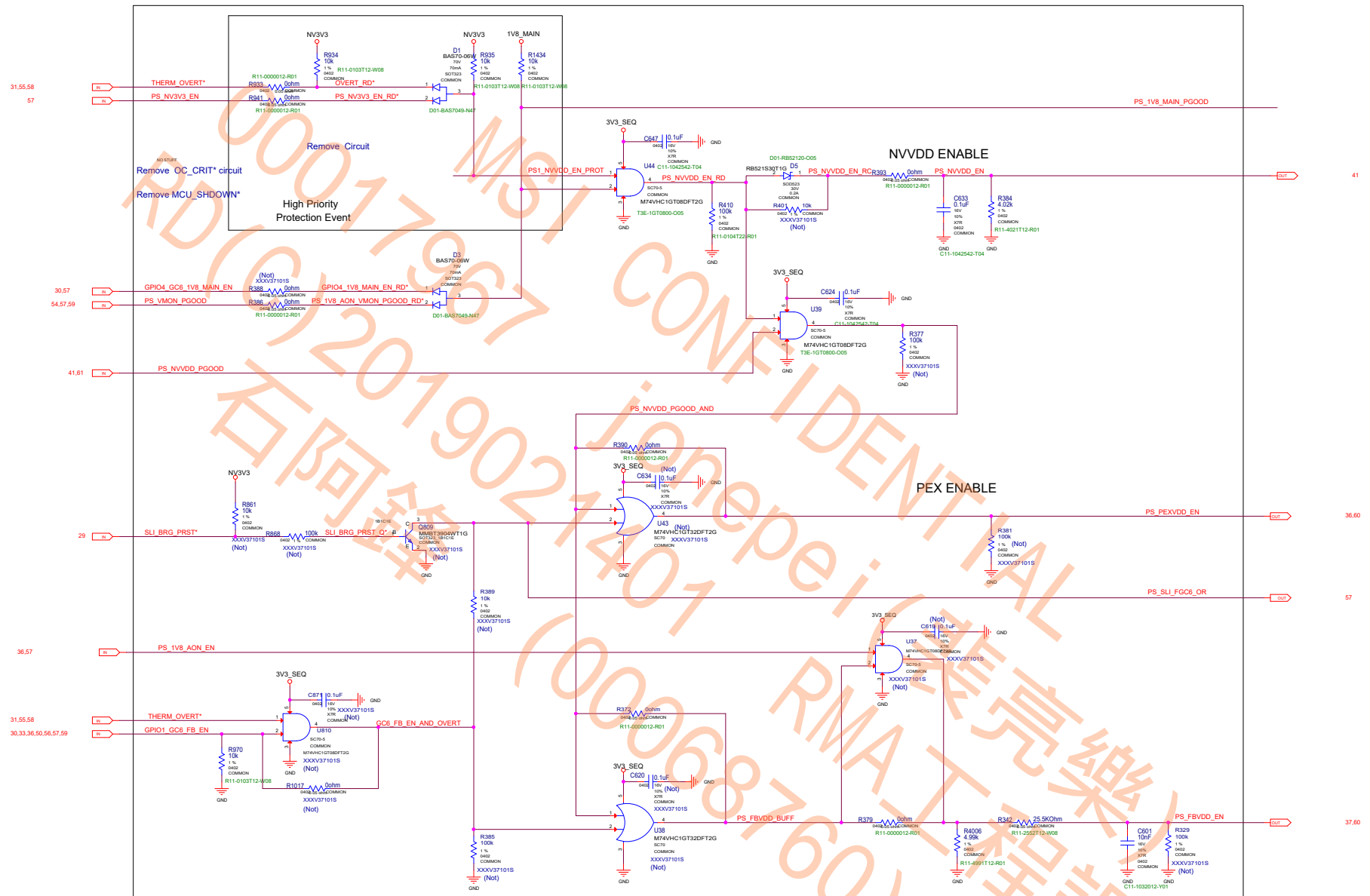
**MICRO-STAR INT'L CO.,LTD**

MS-V377

Size Custom	Document Description <b>5V,1V8,NV3V3 ENABLE</b>	Rev 1.0
Date: Thursday, August 23, 2018		Sheet 57 of 66



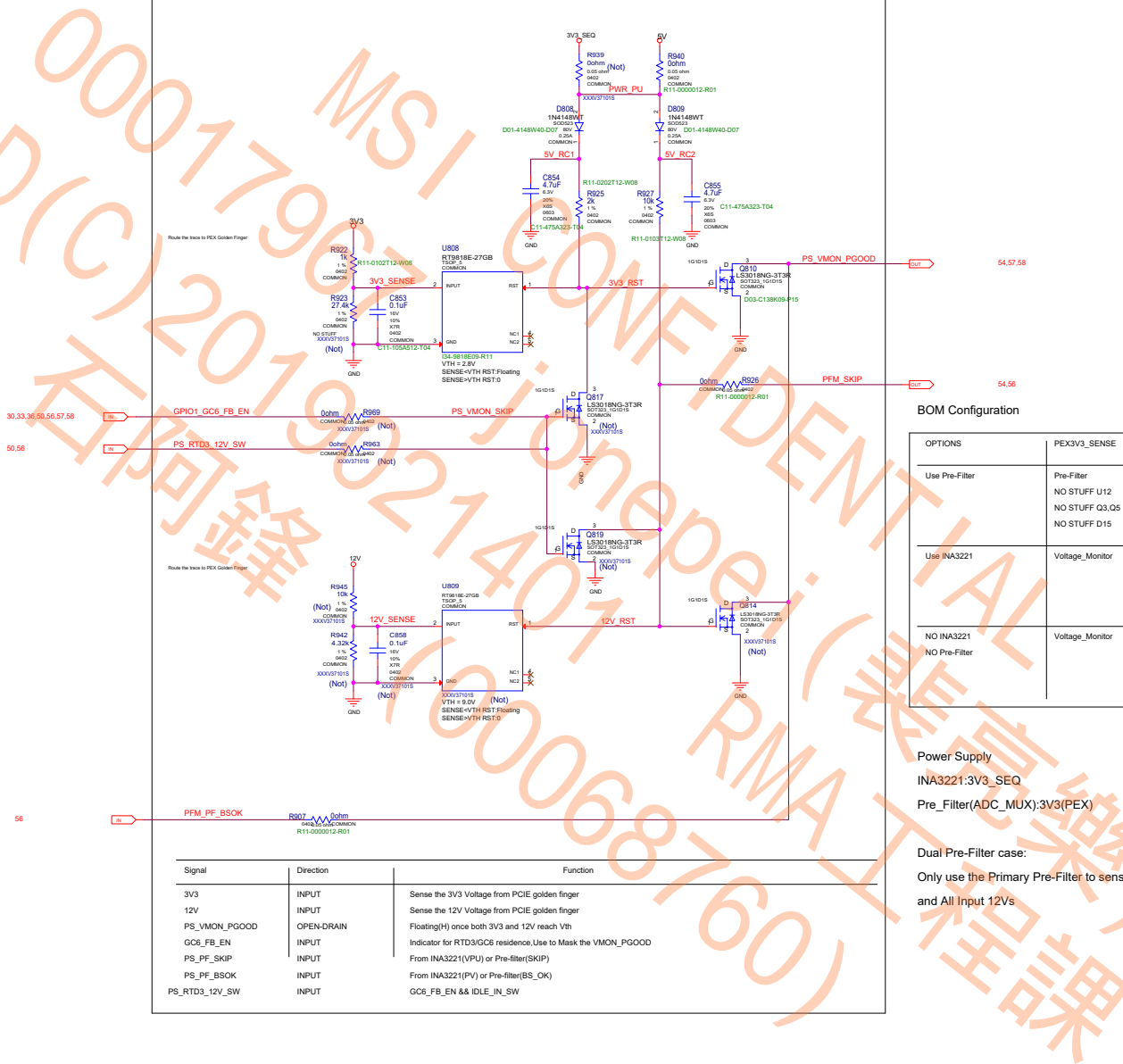
SEQUENCE:NV,PEX,FB ENABLE



**MICRO-STAR INT'L CO.,LTD**  
**MS-V377**

Size Custom	Document Description <b>NV,PEX,FB ENABLE</b>	Rev 1.0
Date: Thursday, August 23, 2018		Sheet 58 of 86





BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3\_SEQ

Pre\_Filter(ADC\_MUX):3V3(PEX)

Dual Pre-Filter case:

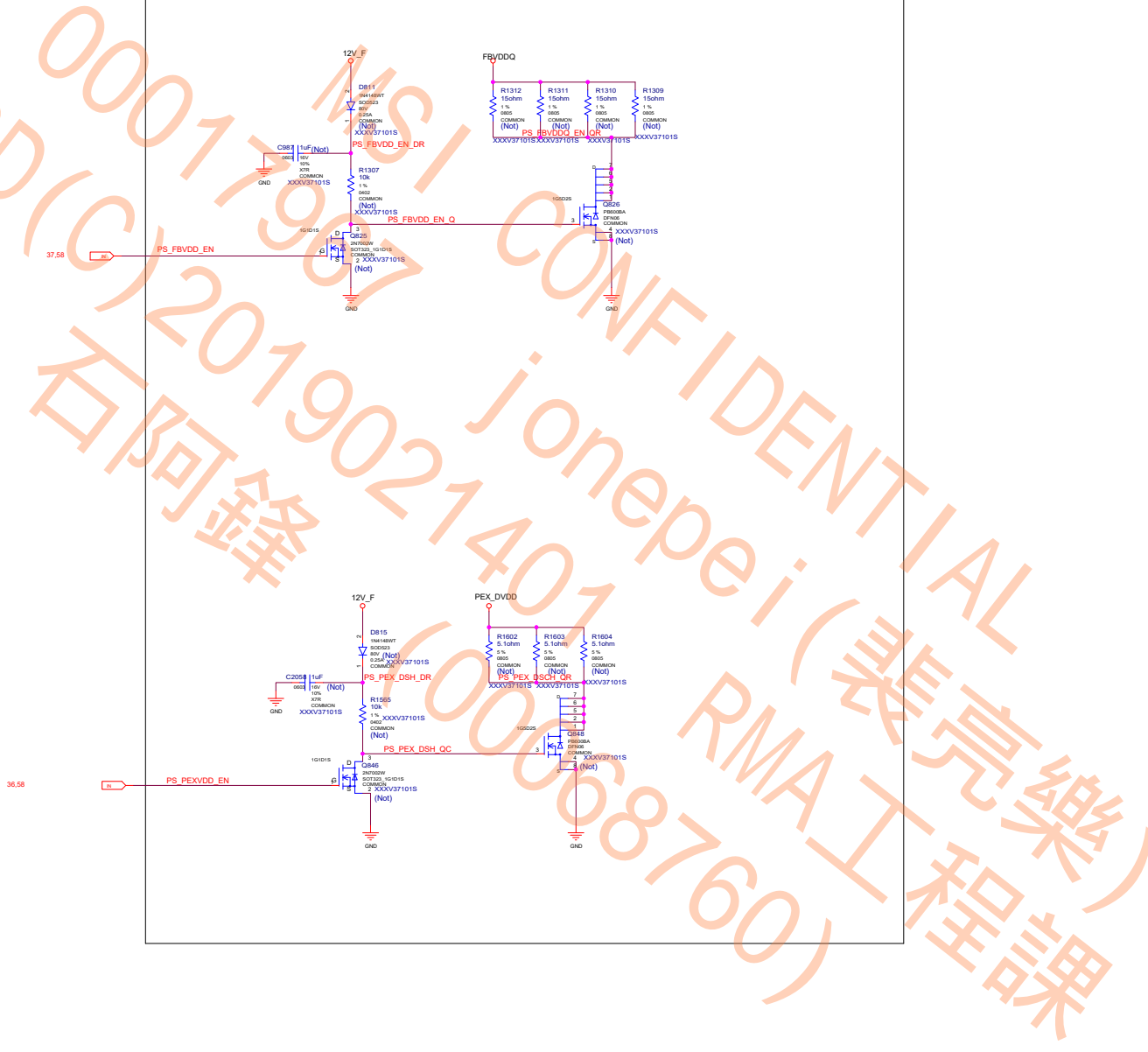
Only use the Primary Pre-Filter to sense 3V3PEX  
and All Input 12Vs

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

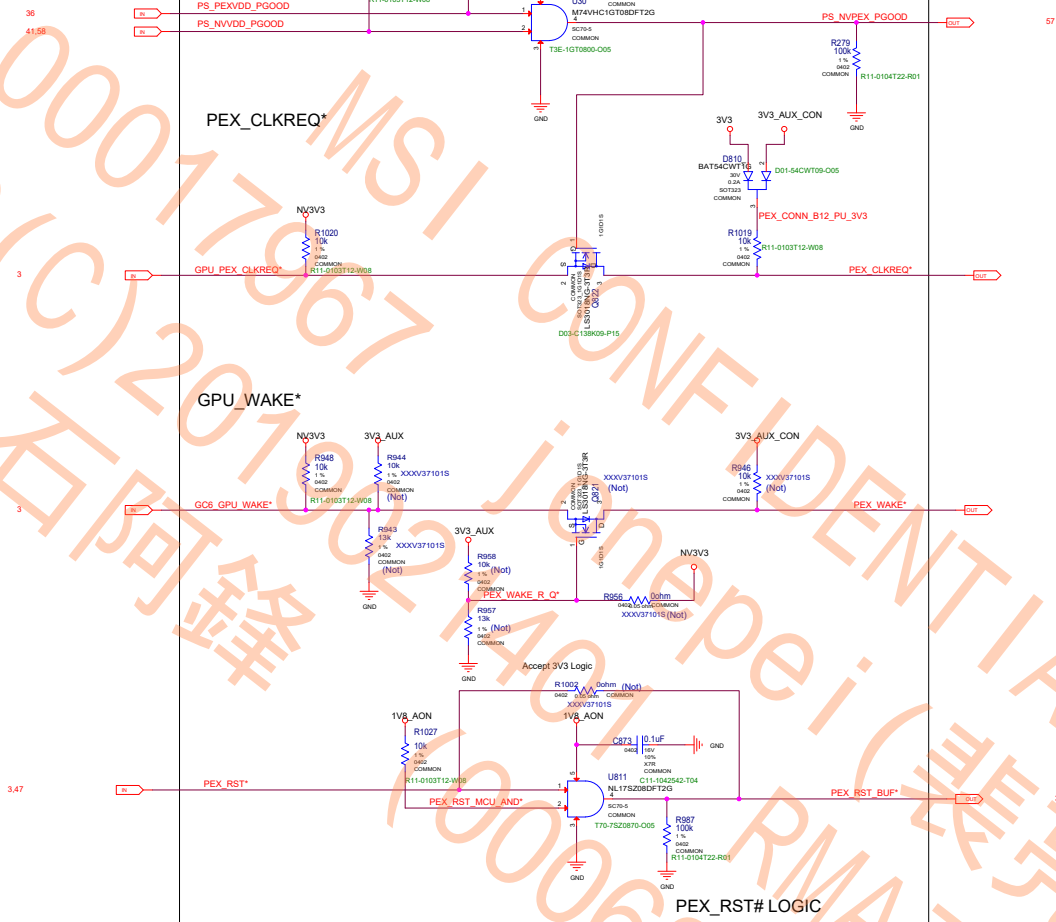
**MICRO-STAR INT'L CO.,LTD**  
**MS-V377**

Size Custom	Document Description <b>PCIE Voltage Monitor</b>	Rev 1.0
Date: Thursday, August 23, 2018		Sheet 59 of 66



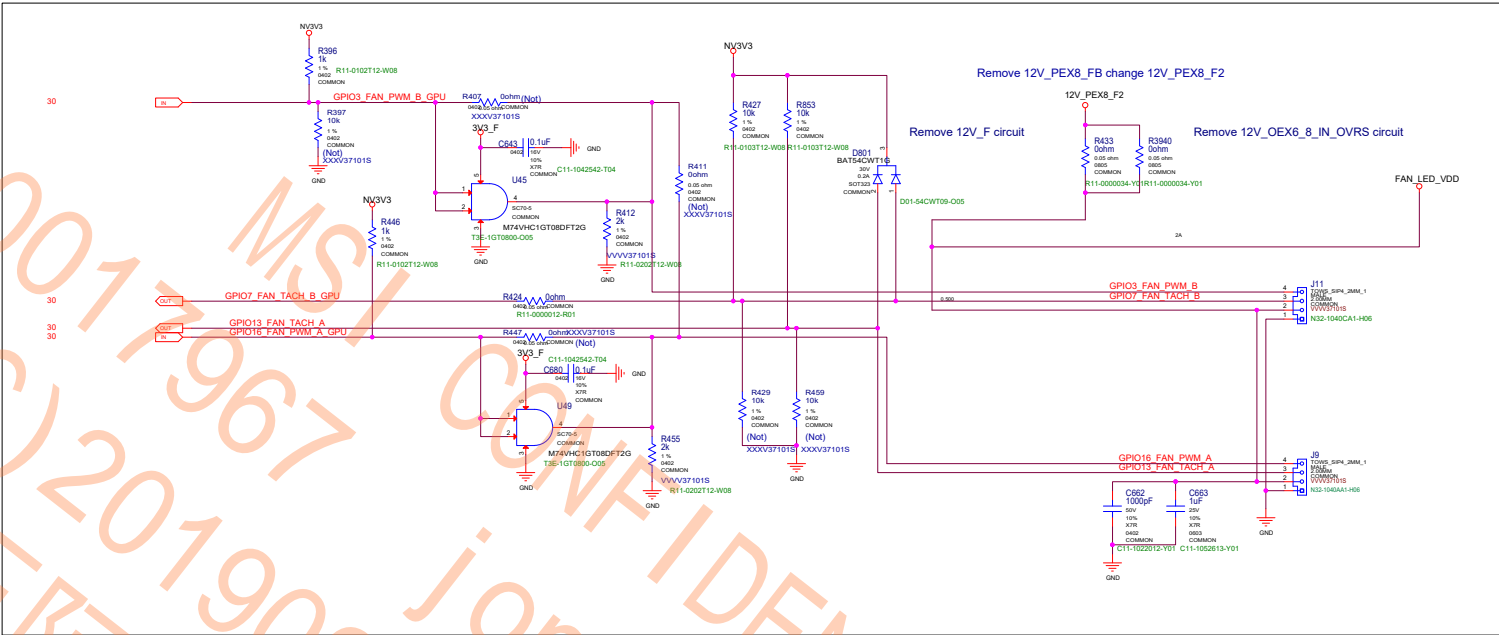








MISC: FAN



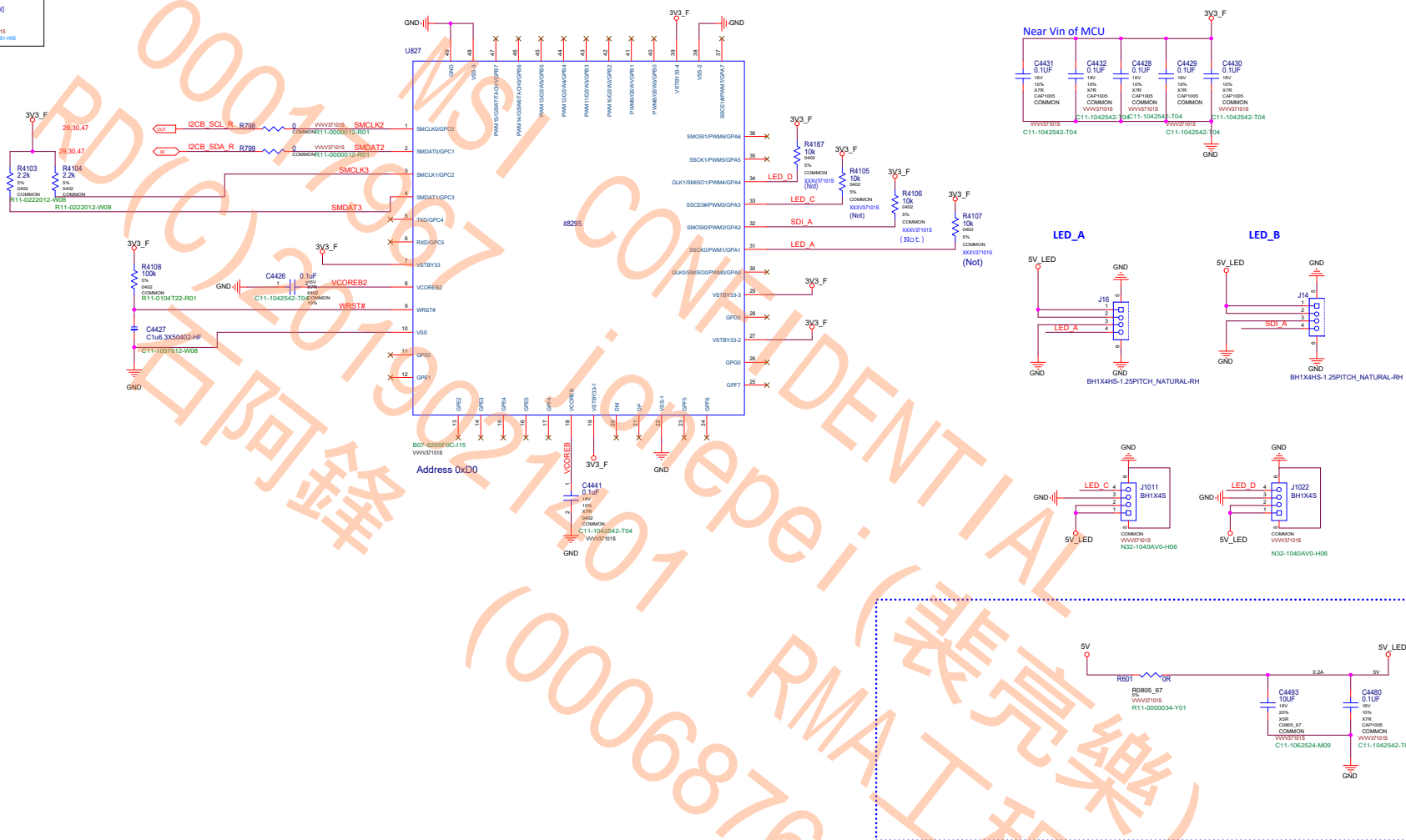
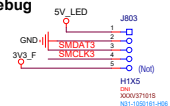
LED BOOST





## Firmware Programming

## Debug

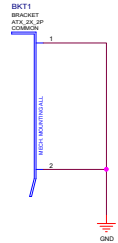




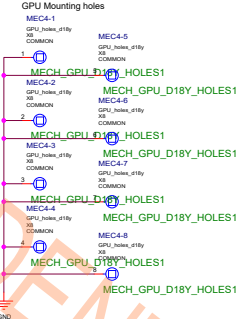
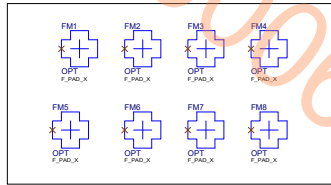
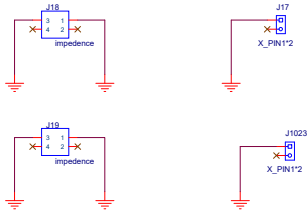
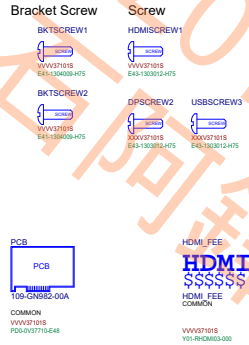
MSI CONFIDENTIAL  
00017967 jonepei (裴亮樂)  
RD(C)2019021401 RMA工程課  
石阿鋒 (00068760)



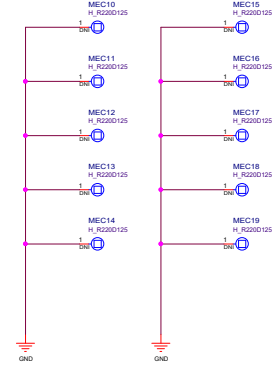
Brackets:



Bracket Screw



Mechanical Holes Symbol





VR THERMAL PROTECTION

41,42,43,44,45



37,39,40